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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1 53(b))

Attorney Docket No. 0756-1943

First Inventor or Application Identifier: Shunpei YAMAZAKI et al.

Title: ELECTRO-OPTICAL DEVICE AND METHOD FOR DRIVING THE SAME

Express Mail Label No.

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. [X] Fee Transmittal Form (e.g., PTO/SB/17)
   (Submit an original, and a duplicate for fee processing)
2. [X] Specification *Total Pages* [53]
   (preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) (35 USC 113) *Total Sheets* [26]
4. [X] Oath or Declaration *Total Pages* [2]
   a. [ ] Newly executed (original or copy)
   b [X] Copy from a prior application (37 CFR 1 63(d))
   (for continuation/divisional with Box 17 completed)
   [Note Box 5 below]
   i. [ ] DELETION OF INVENTOR(S)
   Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1 63(d)(2) and 1 33(b).
5. [X] Incorporation By Reference *(useable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

ADDRESS TO:

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6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission
   (if applicable, all necessary)
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & document(s))
9. [ ] 37 CFR 3 73(b) Statement [ ] Power of Attorney
   (when there is an assignee)
10. [ ] English Translation Document *(if applicable)*
11. [X] Information Disclosure Statement (IDS)/PTO-1449 [X] Copies of IDS Citations
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14. [ ] *Small Entity Statement(s) (PTO/SB/09-12) [ ] Statement filed in prior application, Status still proper and desired
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*A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon.

17. **If a CONTINUING APPLICATION**, *check appropriate box, and supply the requisite information below and in a preliminary amendment*
Divisional of prior application Serial No. 08/912,298, filed July 31 1997; which itself is a Continuation of Serial No. 08/634,382, filed April 18, 1996, now abandoned; which is a Divisional of Serial No. 08/153,080, filed November 16, 1993, now U.S. Patent No. 5,568,288; which is a Divisional of Serial No. 07/857,597, filed March 25, 1992, now U.S. Patent No 5,287,205.
Prior application information: Examiner: J. Dudek Group/Art Unit: 2871

18. CORRESPONDENCE ADDRESS

[ ] Customer Number or Bar Code Label

or [X] Correspondence address below
(Insert Customer No or Attach bar code label here)

Name Eric J Robinson
Firm SIXBEY, FRIEDMAN, LEEDOM & FERGUSON, P C
Address 8180 Greensboro Drive, Suite 800
City McLean State VA Zip Code 22102
Country U S A Telephone (703) 790-9110 FAX (703) 883-0370

Name: Eric J. Robinson Registration No. 38,285

Signature [signature] Date: 7 APRIL 99

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re DIVISIONAL Application of	)	
Shunpei YAMAZAKI et al.	)	
Based On Serial No. 08/912,298	)	Art Unit: 2871
Which Was Filed: July 31, 1997	)	Examiner: J. Dudek
For: ELECTRO-OPTICAL DEVICE AND METHOD FOR DRIVING THE SAME	)	Date: April 7, 1999

PRELIMINARY AMENDMENT

Honorable Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Please preliminarily amend the subject application as follows:

IN THE SPECIFICATION:

Before the first sentence of the specification, insert --This application is a Divisional application of Serial No. 08/912,298, filed July 31 1997; which itself is a Continuation of Serial No. 08/634,382, filed April 18, 1996, now abandoned; which is a Divisional of Serial No. 08/153,080, filed November 16, 1993, now U.S. Patent No. 5,568,288; which is a Divisional of Serial No. 07/857,597, filed March 25, 1992, now U.S. Patent No. 5,287,205.--

REMARKS

This application has been amended to include the continuing application data thereof.

Examination on the merits is requested.

Respectfully submitted,

Eric J. Robinson
Registration No. 38,285

8180 Greensboro Drive, Suite 800
McLean, Virginia 22102
(703) 790-9110

TITLE OF THE INVENTION

ELECTRO-OPTICAL DEVICE AND METHOD FOR DRIVING THE SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an electro-optical device, e.g. to an active liquid crystal electro-optical device, in particular, to a device provided with two complementary thin film insulated gate field effect transistors (hereinafter referred to as C/TFTs) having a structure of modified transfer gate MTG).

Also, the present invention relates to a method for driving an active electro-optical device, in particular, to a method for driving an active electro-optical device with clear gradation level in a digital mode.

2. Description of the Prior Art

An active liquid crystal electro-optical device utilizing TFT is conventionally know. In this device, an amorphous or polycrystalline semiconductor is used for TFT, while either one of conductive type alone is used for each picture element thereof. Namely, an N-channel TFT(referred to as NTFT) is generally linked to the picture element in series.

Since the dielectric constant in a direction parallel to a molecular axis of the liquid crystal composition provided between substrates is different from that in a direction perpendicular thereto due to the material property thereof, arrangement of the composition can easily be made in both directions, horizontally or vertically, to the outside electric field. By utilizing the anisotropy of dielectric constant, the amount of transmitted light or of dispersion thereof is controlled in a liquid crystal electro-optical device, so as to perform ON/OFF display.

Fig.3 shows an electro-optic property of nematic liquid crystal. When the applied voltage is small, which is indicated by

Va or a point A, the amount of transmitted light is approximately 0%, and at Vb or point B, it is approximately 30%, while at Vc or point C, it is approximately 70%, and at Vd or point D, it amounts to approximately 100%. Therefore, when the points A and D alone are used, two-graded display in black-and-white is possible, while, when the points B, C, or the points where electro-optical property (transmittance) rises in Fig.2, are used, the display of intermediate gradation is possible.

As for the conventional electro-optical device utilizing TFTs, gradation display was performed by varying the voltage applied to a gate of the TFT or that applied between source and drain thereof, and controlling the voltage in an analogue mode.

Concerning the conventional method of gradation display in the electro-optical device utilizing TFT, an explanation will be made: an N-channel thin film transistor used for the conventional electro-optical device has the voltage-current characteristic as shown in Fig.3, which shows the voltage-current characteristic of the N-channel thin film transistor utilizing amorphous silicon, and of that utilizing poly-silicon.

By controlling the voltage applied to a gate electrode of the thin film transistor having such characteristic in an analogue mode, drain current can be controlled and therefore strength of the electric field to be applied to the liquid crystal can be varied, whereby gradation display is possible.

In the case of an electro-optical device having picture elements of, for example, 640 x 400 dots, however, it is difficult to manufacture all 256,000 TFTs without variation in characteristics thereof. It is thought that 16 gradation levels are limit of the number of gradation levels of such electro-optical device having 640 x 400 picture elements in order to achieve productivity and yield required for practical process.

A gradation display may be performed by predetermining the

value of gate voltage, while controlling only the turning of ON/OFF by gate voltage, and by variably controlling source or drain voltage. In this case, however, about 18 gradation levels are considered to be a limit, based on the fact that the characteristic are unstable. In an analogue mode of the gradation display control, clear display was difficult due to variation in characteristics of TFT.

Another method of gradation display using multiple frames is suggested. As shown in the outline indicated in Fig.11, when a gradation display is to be performed using, for example 10 frames, by making two frames out of ten transparent, while the remainder of eight frames nontransparent, average 20% of transparency can be displayed at picture element A. A picture element B displays 70% of transparency on an average in the same manner, while a picture element C 50% of transparency on an average.

When such a display is carried out, however, since the number of frame is practically reduced thereby, flickering and display failure were generated. To solve the problem, the increasing of frame frequency, or the like, is suggested, whereas, the increase in power to be consumed in accordance with the increase in driving frequency, as well as the difficulty in the achievement of higher operation speed IC, indicated a limit of this method.

BRIEF SUMMARY OF THE INVENTION

An object of the present invention is to provide a method of compensating the variation in characteristics of TFT by inputting a reference signal repeated in a certain cycle and having signal level which varies during duration of the reference signal, from a controller side, in order to clarify the level of applied voltage, and by controlling the time of connecting the reference

signal to the TFT by digital value, and thereby controlling the voltage to be applied to the TFT, namely, to offer an electro-optical device by using complementary thin film transistors (C/TFTs) having a structure of modified transfer gate (MTG) that performs digital gradation display.

The method is characterized in displaying gradation in an electro-optical device using a display drive method that has a display timing in relation to a time F for writing one picture plane and a time (t) for writing in one picture plane, without changing the time F, by applying a reference signal that has voltage variation in a cycle that is equal to the time (t) to one of the signal lines that are used for drive and selection of a picture element, as well as a selection signal at a certain timing within the time (t), to the other signal line, thereby determining the voltage to be applied to a liquid crystal, and thereby actually applying the voltage to the picture element.

In addition, the method is also characterized in high speed control without being limited by several tens of MHz that was a limit of data transfer speed for a conventional CMOS, since the timing is not dependent upon the transfer of the data, but is processed at a part for signal process. with a high speed clock being added to a driver IC itself that is put on the electro-optical device.

Fig. 1 shows a concrete drive waveform for driving the electro-optical device in accordance with the present invention. The electro-optical device has a circuit configuration equivalent to a circuit diagram having a 2 x 2 matrix form shown in Fig.4. Herein used is a half wave of a sine wave, as the reference signal waveform of varied voltage in a certain period of time as described supra. Sine waves 309, 310 are applied to V_{DD1}303, V_{DD2}304 that fall in a direction of a scanning line, while two-polarity (hereinafter referred to as bipolar) signals are applied

to V_{GG1}301, V_{GG2}302 that fall in a direction of information line. Digital control is carried out by a timing of applying the bipolar signals.

Namely, the amount of charge to be accumulated at the point A as well as electric potential at the point A are determined by changing the timing for selecting the signal of varied voltage in a certain period of time, as shown in 309 and 310, and the size of the electric field to be applied to the picture element as well as to the liquid crystal is determined by defining a certain value for the electric potential 313 of a counter electrode.

The timing of applying the bipolar signal to gate signal lines such as V_{GG1}, V_{GG2} is not determined by the transfer speed of the information signal, but is regulated by the reference clock input to the driver IC that is directly connected to the electro-optical device in the present invention. Namely, in the case of an electro-optical device of 640 x 400 dots, drive frequency is approximately 20MHz based on the limitation of CMOS, and, in order to calculate the number of gradation levels by utilizing this value, the drive frequency is to be indicated as a product of the number of scanning lines, the number of frames, the bipolar pulse, and the number of gradation levels, from which 20MHz is divided by (400 x 60 x 2), to obtain the number of gradation levels which is 416, and it is needless to say that a display having 832 gradation levels is possible by dividing the display screen into two.

The present invention is characterized in performing gradation display in a digital method, instead of employing the conventional analogue method of gradation display. To obtain the effect, in the case of an electro-optical device having picture elements of 640 x 400 dots, it is very difficult to eliminate the variation in characteristics for all the TFTs of 256,000, at the time of manufacturing, and, practically, in consideration of

mass production and yield, 18 gradation display is supposed to be a limit, whereas, the method of compensating the variation in characteristics of TFTs is employed in the present invention by inputting a reference signal from a controller side, in order to clarify the level of applied voltage, and by controlling the timing of connecting the reference signal to TFT by digital value, and thus controlling the voltage to be applied to TFT, which allows for clear digital gradation display.

Also, clear digital gradation display is possible without changing the number of frames for one picture plane, by defining two kinds of drive frequency, whereby the generation of flickering concomitant with the decrease in the number of frames can be prevented.

For example. when a gradation display is performed in a normal analogue mode for an electro-optical device, for which 256,000 pairs of TFTs of 640 x 400 dots are formed in 300nm square, a 16-gradation display is an upper limit due to the variation in TFT characteristics of approximately ±10%. In the case of digital gradation display in accordance with the present invention, however, since the variation in characteristics of TFT devices can be compensated, a 256-gradation display is possible, and a various and subtle color display of as many as 16,777,216 kinds of colors are possible thereby. When a software such as a television image is to be projected on the screen, for example, the projection of a ''rock'' scene of the same color requires subtle difference in colors due to the existence of slight recesses and the like thereon, and the 16-gradation display is not suitable for the display as close to the natural coloration ion as possible. However, the subtle variation in tone can be displayed by the gradation display in accordance with the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of the invention and together with the description, serve to explain the principle of the invention.

Fig. 1 shows an example of a drive waveform in accordance with the present invention.

Fig.2 shows an electric photo-optical characteristic of the conventional electro-optical device.

Fig.3 shows a current-voltage characteristic of TFT in the case poly-silicon and amorphous silicon are adopted as materials used for the TFT.

Fig.4 shows an example of a circuit of an active matrix electro-optical device applicable to the present invention, subject to a part of 2 x 2 matrix structure.

Fig.5 shows an example of a circuit of an active matrix electro-optical device applicable to the present invention, subject to a part of 2 x 2 matrix structure.

Fig.6 corresponding to Fig.5 shows the arrangement of an active matrix electro-optical device applicable to the present invention.

Figs.7(A) to (I) corresponding to the first preferred embodiment, show schematic cross sectional views indicating the manufacturing process of the TFT applicable to the present invention.

Fig.8 and Fig.9 show schematic structure of the display device applicable to the electro-optical device described in the present invention.

Fig. 10 shows a system structure of a drive circuit for an electro-optical device applicable to the present invention.

Fig.11 shows a concept of gradation display in accordance with the conventional method.

Fig.12 shows the manufacturing process of forming a color

filter on the substrate of the electro-optical device.

Fig.13 corresponding to the third preferred embodiment. shows the arrangement of an active matrix electro-optical device applicable to the present invention.

Figs.14(A) to (G) corresponding to the second preferred embodiment, show schematic cross sectional views indicating the manufacturing process of the TFT applicable to the present invention.

Fig.15 shows an example of a drive waveform in accordance with the present invention.

Fig.16 shows an example of application I the electro-optical device in accordance with the present invention, to a view finder.

Fig.17 shows an example of the electro-optical device in accordance with the present invention, of a front type projection television.

Fig.18 shows a schematic structure of the electro-cptical device in accordance with the present invention.

Fig.19 shows a system structure of a drive circuit of the electro-optical device applicable to the present invention.

Fig.20 shows an example of the application of the electro-optical device in accordance with the present invention, to a personal computer.

Fig.21 corresponding to the third preferred embodiment, shows the arrangement of the active matrix electro-optical device applicable to the present invention.

Figs.22 (A) to (G) corresponding to the third preferred embodiment, show schematic cross sectional views indicating the manufacturing process of the TFT applicable to the present invention.

Fig.23 is a circuit diagram showing an equivalent circuit in accordance with the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred Embodiment 1

In this embodiment, a wall television is manufactured by using the liquid crystal display device having the circuit structure as shown in Fig.5, which will be described infra. The manufacturing process of the TFT employed as an active device of the electro-optical device is shown in Figs. 7 (A) through (I). Polycrystalline silicon that is subjected to laser annealing process is used as a semiconductor material that forms the TFT.

The arrangement of the electrode, etc. of the actual electro-optical device corresponding to the circuit structure is shown in Fig.6, which shows only a part corresponding to 2 x 2 or less thereof for simplification. The drive signal waveform that is actually used therefor is shown in Fig.1, which also shows the signal waveform of 2 x 2 matrix form for simplification.

Referring to Fig.7, the manufacture of the liquid crystal panel used in accordance with the preferred embodiment 1 will be described. Referring to Fig.7(A), a silicon oxide film is manufactured to a thickness of 1000-3000 angstroms as a blocking layer 51, by magnetron RF (high frequency) sputtering, on the glass 50, which is not expensive, and which endure the heat treatment of not more than 700 °C, e.g. of approximately 600 °C, under the process condition of oxygen 100% atmosphere, deposition temperature of 15 °C, output of 400 to 800W, and the pressure of 0.5Pa. The deposition rate was 30 to 100 angstroms/minute when quartz or single crystalline silicon was used as a target.

An intrinsic. or substantially intrinsic silicon film 52 was manufactured by plasma CVD thereupon. The deposition temperature ranged from 250°C to 350 °C, and it was 320 °C in

the preferred embodiment 1, using mono-silane (SiH_4) as a reactive gas, which can be replaced with disilane (Si_2H_6) or trisilane (Si_3H_8). These were introduced in a PCVD device, and deposition was carried out by applying high frequency power of 13.56MHz under the pressure of 3Pa. The suitable high frequency power is 0.02 to 0.10W/cm^2, while 0.055W/cm^2 was adopted in the preferred embodiment 1. The flow of mono-silane (SiH_4) was 20SCCM, and the deposition rate at the time was approximately 120 angstroms/minute. Boron can be added to the deposited film at a concentration of 1 x 10^{15} to 1 x 10^{18}cm^{-3} using diborane during the deposition, in order to control the threshold voltage (Vth) almost equal between PTFT and NTFT. Sputtering or low pressure CVD can be employed instead of the plasma CVD for the deposition of the silicon layer that will be a channel region of TFT, and the methods will be described below in simplified manner.

In the case of sputtering, the back pressure before sputtering was no more than 1 x 10^{-5} Pa, and the sputtering was performed using a single crystalline silicon as a target, in the atmosphere in which 20-80% of hydrogen was added to argon: e.g. 20% of argon and 80% of hydrogen. The deposition temperature was 150°C, and the frequency was 13.56MHz, while the sputtering output was 400-800W, and the pressure was 0.5Pa. In the case of low pressure CVD, deposition was carried out by supplying disilane (Si_2H_6) or trisilane(Si_3H_8) to a CVD device, at a temperature of 450-550 °C, 100 to 200°C lower than that for crystallization, e.g. at 530 °C. The pressure inside of the reactor was 30-300Pa, while the deposition rate was 50-250 angstroms/minute.

Oxygen in the film formed in these manner is preferably not more than 5 x 10^{21}atoms·cm^{-3}. It is preferred that the oxygen concentration be not more than 7 x 10^{19} atoms·cm^{-3},

desirably no more than 1 x 10^{19}atoms·cm^{-3}, in order to promote crystallization, however, if it is too low, current leakage under the OFF condition of TFT is increased due to the illumination of the back light of the electro-optical device, whereas, if it is too high, crystallization becomes difficult, and thus laser annealing temperature must be increased or the laser annealing time must be prolonged. The concentration of hydrogen was 4 x 10^{20}atoms·cm^{-3}, and is one atom% compared to the silicon supposed to be 4 x 10^{22}atoms·cm^{-3}.

The oxygen concentration can be not more than 7 x 10^{19}atoms·cm^{-3} or desirably no more than 1 x 10^{19} atoms·cm^{-3}, so as to promote crystallization with regard to source or drain and oxygen can be added only to the channel forming region of the TFT that forms pixel, at concentrations of 5 x 10^{20} to 5 x 10^{21}atoms·cm^{-3} by ion implantation.

A silicon film an amorphous condition was formed at 500 to 5000 angstroms in the above-mentioned manner, and at 1000 angstroms in the preferred embodiment 1.

Referring to Fig.7 (B), a photoresist pattern 53 is formed with openings formed only on the source and drain regions in the photoresist pattern using a mask P1. A silicon film 54 was manufactured thereon, which is to be an n-type activation layer, by plasma CVD, at the deposition temperature of 250°C to 350°C, e.g. 320°C in the preferred embodiment 1, using mono-silane (SiH_4) and 3% concentration of phosphine (PH_3) of mono-silane base. These were introduced in the PCVD device at a pressure of 5Pa, and the deposition was carried out by applying a high frequency power of 13.56MHz. The suitable high frequency power is 0.05-0.20W/cm^2, and it was 0.120W/cm^2 in the preferred embodiment 1.

The electric conductivity of the n-type silicon layer formed in the above-mentioned manner was approximately 2 x 10^{-1}[$(\Omega\cdot cm)^{-1}$],

while the film thickness was 50 angstroms. The resist 63 was then removed by lift-off method, so as to form source, drain regions 55, 56.

A p-type silicon semiconductor layer was formed using the same process. Mono-silane (SiH_4) and 5% concentration of diborane(B_2H_6) of mono-silane base were used as the introduction gas. These were introduced in the PCVD device at a pressure of 4Pa, and deposition was carried out by applying a high frequency power of 13.56MHz. The suitable high frequency power is 0.05 to 0.80W/cm^2, and 0.120W/cm^2 was adopted in the preferred embodiment 1. The electric conductivity of the p-type silicon layer formed in this manner was approximately 5 x 10^{-2} [$(\Omega \cdot cm)^{-1}$], while the film thickness was 50 angstroms. Source, drain regions 59, 60, were formed by using the lift-off method in the same manner as the n-type region. The silicon film 52 was then etched off, using a mask P3, and an island region 63 for N-channel thin film transistor as well as an island region 64 for P channel thin film transistor were formed.

The source, drain and channel regions were laser-annealed using XeCl excimer laser, while a laser doping was carried out to the activation layer. As for the laser energy at the time, a threshold energy was 130mJ/cm^2, whereas 220mJ/cm^2 was required so as to melt the entire film thickness. When the energy of no less than 220mJ/cm^2 is irradiated from the start, hydrogen included in the film is abruptly ejected, whereby the film is damaged. For that reason, melting has to be carried out after the hydrogen is primarily purged at a low energy. In the preferred embodiment 1. after the hydrogen was at first purged at 150mJ/cm^2, crystallization was carried out at 230mJ/cm^2.

By the annealing, the silicon film is transformed from an amorphous structure to the state of higher order, with a part thereof being crystallized. In particular, a relatively higher

order region of the silicon coated film tends to be crystallized into a crystalline region by the annealing. However, silicon atoms are pulled with each other since bonds are formed between such regions by silicon atoms existing therebetween. Laser Raman Spectroscopy results show a peak shifted to the fraquency lower than the single crystalline silicon peak of 522cm^{-1}. The apparent grain diameter was calculated 50 to 500A, based on a half band width, however, in fact, the film comprises a lot of high crystalline regions which constitute a cluster structure, and clusters are anchored to each other in the film by bonds between silicon atoms.

As a result, it can be said that substantially no grain boundary (hereinafter referred to as GB) exists in the film. Since carriers can easily move between the respective clusters, through the anchored portions, a carrier mobility higher than that of a poly-crystalline silicon in which a GB obviously exists, is achieved. Namely, Hall mobility (μh) of 10-200cm^2/Vsec, electron mobility (μh) of 15-300cm^2 /VSec can be obtained.

A silicon oxide film was formed as a gate insulating film thereon in the thickness ranging from 500 to 2000A, e.g., at 1000A, under the same condition as that for the manufacturing of the silicon oxide film as a blocking layer. At the time of forming the film, a small amount of fluorine may be added thereto, so as to stabilize sodium ion.

Further, on the upper surface thereof, a silicon film doped with phosphorus at 1 to 5 x 10^{21}atoms·cm^{-3}, or a multi-layered film comprising this silicon film and molybdenum (Mo), tungsten (W), $MoSi_2$ or WSi_2 film formed thereupon, was formed, which was then subjected to a patterning process using a fourth photomask P4, and the structure shown in Fig.7(E) was thereby obtained. A gate electrode 86 for NTFT, as well as a gate electrode 87 for

PTFT were formed: e.g. a channel length of 7μm; and as a gate electrode P-doped Si of 0.2μm on which molybdenum was formed at 0.3μm.

In the case aluminum (Al) is used as a gate electrode material, after patterning the gate electrode material by a fourth photomask 69, anodic oxidation can be applied to the surface thereof. In this case, a self-aligning process can be employed, whereby the contact hole of a source and drain can be formed closer to the gate, and the TFT characteristic can be further improved thereby, due to the improved mobility as well as the reduction in threshold voltage.

In this way, C/TFT can be manufactured without elevating the temperature not less than 400°C, in every process. Therefore, it is not necessary to use an expensive material such as quartz for the substrate, and it can be said that this is a most suitable process for manufacturing the wide-screen liquid crystal display device in accordance with the present invention.

Referring to Fig.7(F), an inter-layer insulating material 68 was sputtered, so as to form a silicon oxide film, in the manner described supra. The silicon oxide film can be formed by LPCVD, photo-CVD, or by atmospheric pressure CVD, at a thickness of, for example, 0.2 to 0.6μm, and thereafter, an opening 78 for electrode was formed using a fifth photomask P5. In addition, after aluminum was formed by sputtering at a thickness of 0.3μm thereupon, while a lead 74 as well as contacts 73, 75 were manufactured using a sixth photomask P6, an organic resin 77 for flattening, for example, a translucent polyimide resin was applied to and formed on the surface, and an opening for electrode was formed again by a seventh photomask P7. An ITO (indium tin oxide) was formed on the surface thereof, at a thickness of 0.1μm by sputtering, and a picture element electrode 71 was formed using an eighth photomask P8. The ITO was formed at

a temperature ranging from room temperature to 150 °C, and was subjected to annealing process at 200-400 °C in oxygen or atmosphere.

The electric characteristics of P-TFT thus obtained were: mobility of 40(cm^2 /Vsec), Vth of -5.9(V), while those of NTFT were: mobility of 80(cm^2/Vsec), and Vth of 5.0(V).

In this manner, one substrate for the electro-optical device manufactured in accordance with the present invention, was obtained.

The wirings of the electrode, etc., of the liquid crystal display device are shown in Fig. 6. An N-channel thin film transistor and a P-channel thin film transistor are provided on the intersection of a first signal line 3 and a second signal line 4, whereby the device has a matrix structure with the use of a modified TG type C/TFT. TFT 13 i connected to the second signal line 4 through a contact of an input terminal of a drain 10, while a gate 9 is connected to the first signal line 3. The output terminal of a source 12 is connected to an electrode 17 of the picture element through a contact.

On the other hand, regarding PTFT 22, the input terminal of a drain 20 is connected to the second signal line 4 through a contact, while a gate 21 is connected to the signal line 3, and the output terminal of a source 16, to the picture element electrode 17 through a contact, in the same manner as NTFT. By repeating such a structure horizontally and vertically, the liquid crystal display device having picture elements as many as 640 x 480, 1280 x 960, or 1920 x 400 in this embodiment, can be obtained.

In this way, a first substrate of a pair of substrates was obtained.

The manufacturing method of the other, or a second substrate is shown in Fig.12. A striped color filter is provided on the

substrate corresponding to each picture element. The polyimide resin mixed with black pigment was formed on a glass substrate at a thickness of 1μm, by spin coating, and a black stripe 81 was formed using a ninth photomask P9. Then, the polyimide resin mixed with a red pigment was formed at 1μm by spin-coating, and a red filter 83 was formed using a tenth photomask P10. A green filter 85 and a blue filter 86 were formed in the same manner, using masks P11, P12. Each filter was baked in nitrogen for sixty minutes, at a temperature of 350 °C during the manufacture thereof. A leveling layer 89 was then manufactured using transparent polyimide, again by spin coating.

An ITO (indium tin oxide) was then formed on the entire filter at a thickness of 0.1μm by sputtering, and a common electrode 90 was formed using a fifth photomask P13. The ITO was formed at a temperature ranging from room temperature to 150 °C, and was subjected to the annealing process at 200 to300 °C in oxygen or atmosphere, so as to obtain a color filter layer and the electrode 90 on the second substrate.

A polyimide precursor was printed on the substrate by an offset method, was baked in a non-oxidating atmosphere, e.g. in nitrogen, for an hour, at a temperature of 350 °C, and was subjected to a known rubbing method, whereby the surface condition of the polyimide was changed, and a means to allow for a liquid crystal molecule to be oriented in a certain direction at least in the initial stage was provided.

The nematic liquid crystal composition was sandwiched by the first and the second substrates as described above. The periphery of the first and the second substrates is fixed with an epoxy adhesive. A TAB shaped driving IC and a PCB comprising common signal and electric potential wirings are connected to leads provided on the substrate, and a polarizing plate was attached to the outside thereof, so as to obtain a transmission

type electro-optical device.

A schematic diagram of the electro-optical device in accordance with this embodiment is shown in Figs. 8 and 9. The liquid crystal panel 220 manufactured in the processes described above was installed by combining it with a rear part lighting device 221 comprising three pieces of cold cathode tubes arranged thereon, and was then connected to a tuner 223 for receiving television radio wave, so as to complete the electro-optical device. Since the device has a flat shape compared with the conventional one of CRT type, it can be installed on the wall, and the like.

Referring to Fig.10, the driving peripheral circuit of the electro-optical device in accordance with the present invention will be explained:

A driving circuit 352 is connected to the wirings 350, 351 on the side of an information signal, connected to the matrix circuit of the electro-optical device. The driving circuit 352 comprises two parts when divided by a driving frequency system, i.e. one is a data latch circuit system 353, which is the same as in the conventionally known driving method, and which primarily comprises a basic clock CLK signal circuit 355 for transferring the signals of a data signal circuit 356 in order, performing one bit to twelve bits parallel processing. The other is a part in accordance with the present invention, and comprises a clock 357 corresponding to the degree of division necessary for gradation display, a flip flop circuit 358, and a counter 360. The counter 360 forms a bipolar pulse generation timing corresponding to the gradation display data sent from the data latch system 353. Further, the gradation display data can be controlled in finer way, when a ROM table for converting Δt into sinθ is used between the exit of the latch circuit and a data line 361.

The present invention is characterized in that the clear

digital gradation display is possible without changing the number of frames for re-writing the screen, by taking two kinds of driving frequencies. The generation of flickering and the like caused by the decrease in the number of frames can be prevented thereby.

On the other hand, a driving circuit 364 connected to signal lines 363, 362 on a scanning side controls the sine wave transmitted from a sine wave oscillating circuit 365 by a flip flop circuit 366 of a clock CLK 367, and the select signal is applied to the signal lines 363, 362.

By digitally controlling the timing for cutting the sine wave signal on the scanning side by the bipolar pulse on the information side, gradation display is possible.

When an analogue gradation display is carried out in a normal mode for the electro-optical device comprising, for example, 768,000 pairs of TFTs of 1920 x 400 dots formed into a 300mm square, the variation in characteristics of the TFTs becomes ±10% as a whole, and thus a gradation display having 16 gradation levels is an upper limit, whereas. when a digital gradation display is carried out in accordance with the present invention, it is hardly affected by the variation in characteristics of TFTs, and a gradation display having 64 gradation levels is thus possible for the electro-optical device of the same size, while various and subtle expression of 262,144 kinds of colors is achieved in color display.

Preferred Embodiment 2

The formation of a view finder for a video camera utilizing an electro-optical device having a diagonal of one inch in accordance with this second preferred embodiment 2 will be described below.

In this embodiment, the number of picture elements was 387 x 128, and the device was formed using a high mobility TFT obtained by a low temperature process, so as to form the view finder. The arrangement of the active device on the substrate of the liquid crystal display device used in this embodiment is shown in Fig. 13, and the manufacturing process of the TFT part is shown in Fig.14 in such a way that each corresponds to A-A' cross section and B-B' cross section shown in Fig.13. Referring to Fig.14(A), a silicon oxide film is manufactured at a thickness of 1000 to 3000A as a blocking layer 51 by magnetron RF(high frequency) sputtering, on the inexpensive glass substrate 50 that bears heat treatment of no more than 700 °C, e.g. approximately 600 °C. The conditions for the process are: 100% oxygen atmosphere, formation temperature of 15 °C, output of 400 to 800W, and pressure was 0.5Pa. The formation rate using quartz or single crystalline silicon as a target was 30 to 100Å/min.

A silicon film was then formed thereon by LPCVD(low pressure chemical vapor deposition), sputtering, or by plasma CVD. When the low pressure chemical vapor deposition was employed, film formation was carried out by supplying disilane (Si_2H_6) or trisilane (Si_3H_8) to a CVD device, at a temperature of 450 to 550 °C, 100 to 200 °C lower than the temperature for crystallization, e.g. at 530 °C. The pressure in a reactor was 30 to 300Pa, while the film formation rate was 50 to 250Å/min. Boron may be added to the film using diborane at a concentration of 1×10^{15} to 1×10^{18} atoms·cm^{-3}, during the manufacture thereof, in order to control the threshold voltages (Vth) for PTFT and NTFT almost of the same.

In the case of the silicon film formation by sputtering, the back pressure before sputtering was not more than 1×10^{-5}Pa, and the formation was carried out in the atmosphere comprising 20 to 80% of hydrogen mixed with argon; e.g. argon 20% and hydrogen

80%, using single crystalline silicon as a target. The formation temperature was 150 °C, and the frequency of high frequency power applied thereto was 13.56MHz, sputtering output was 400 to 800W, and the pressure was 0.5Pa.

Silicon film formation by plasma CVD was carried out at a temperature of, for example, 300 °C, using mono-silane(SiH_4) or disilane(Si_2H_6), which were introduced in a PCVD device, and high frequency power of 13.56MHz was applied thereto, so as to carry out film formation.

Oxygen in the film formed by these methods is preferably not more than 5 x $10^{21}cm^{-3}$. If the oxygen concentration is too high, crystallization is hard to occur, and the temperature of thermal annealing has to be elevated, or else, the time of thermal annealing has to be longer. If the concentration is too low, the leakage current in an OFF state is increased due to the back light. For that reason, the concentration range was defined from 4 x 10^{19} to 4 x $10^{21}atoms \cdot cm^{-3}$. Hydrogen concentration was 4 x $10^{20}atoms \cdot cm^{-3}$, or one atom% compared to the silicon of 4 x $10^{22}atoms \cdot cm^{-3}$.

After a silicon film is amorphous state was manufactured at a thickness of 500 to 5000Å, e.g. at 1500 Å, in the manner described above, middle temperature heat treatment was carried out in a non-oxidating atmosphere at a temperature of 450 to 700 °C, for 12 to 70 hours, for example, the film was maintained at a temperature of 600 °C in a hydrogen atmosphere. Since the silicon oxide film is amorphous structure is formed on the substrate surface under the silicon film, a specific nucleus does not exist due to the heat treatment, and the entire body is uniformly thermal-annealed. Namely, amorphous structure is retained during the manufacture of the film, and hydrogen is simply mixed therein.

The silicon film was transformed from the amorphous

structure into the state of higher order, through the annealing, with a part thereof being crystallized. In particular, a relatively higher order region of the silicon coated film tends to be crystallized into a crystalline region by the annealing. However, silicon atom are pulled with each other since bonds are formed between such regions by silicon atoms existing therebetween. Laser Raman Spectroscopy results show a peak shifted to the frequency lower than the single crystal silicon peak of 522cm^{-1}. The apparent grain diameter thereof is calculated 50-500A, based on a half band width, seemingly like the case of a micro-crystal, however, actually, a film in semi-amorphous structure was formed including therein high crystalline regions constituting a cluster structure, clusters being anchored to each other by bonds between silicon atoms.

As a result, it can be said that substantially no GB exits in the film. Since carriers can easily move between each cluster through the anchored portions, mobility higher than that of polycrystalline silicon in which GB obviously exists, is obtained. Namely, Hall mobility (μh) of 10 to 200cm^2/Vsec, electron mobility (μe) of 15 to 300cm^2/Vsec can be obtained.

When polycrystallization of the film is carried out by high temperature annealing process at 900-1200 °C, instead of the above-mentioned middle temperature annealing process, segregation of impurities in the film occurs due to the solid growth from nucleus, whereby impurities such as oxygen, carbon, nitrogen are increased in the GB, and, although the mobility in crystal is higher, the movement of carriers is hindered by a barrier formed by the GB. Consequently, the mobility no less than 10 cm^2/Vsec cannot be achieved in practice. From that reason, the silicon semiconductor having semi-amorphous or semi-crystalline structure is used in this embodiment.

Referring to Fig.14(A), a silicon film is photo-etched by a

first photomask P14, and a region 13 (channel width of 20μm for NTFT was manufactured on the side of the A-A' cross section shown in the figure, while a region 22 for PTFT on the side of B-B' cross section.

A silicon oxide film was formed thereon at a thickness of 500 to 2000Å, e.g. at 1000Å, as a gate insulating film. The manufacture thereof was carried out under the same conditions for those applied for the manufacture of the silicon oxide film as a blocking layer. A small amount of fluorine may be added during the manufacture thereof, so as to stabilize sodium ion.

On the upper surface thereof, a silicon film doped with phosphorus at 1 to 5 x 10^{21}atoms·cm^{-3}, or a multi-layered film comprising this silicon film and molybdenum (Mo), tungsten (W), $MoSi_2$ or WSi_2 film formed thereupon, was formed, which was then subjected to a patterning process using a second photomask P15, and the structure shown in Fig.14(B) was thereby obtained. A gate electrode 9 for NTFT, as well as a gate electrode 21 for PTFT were formed. In this embodiment, as a gate electrode P-doped Si of 0.2μm and molybdenum of 0.3μm thereon were formed and channel length of the NTFT was 10μm and channel length of the PTFT was 7μm. Referring to Fig.14(C), boron was ion-doped at a dose of 1 to 5 x $10^{15}cm^{-2}$, to a source 18 and a drain 20 for PTFT. Referring to Fig.14(D), then, a photoresist 61 was formed using a photomask P16. Phosphorus was ion-doped at a dose of 1 to 5 x $10^{15}cm^{-2}$, as a source 10 and a drain 12 for NTFT.

In the case aluminum (Al) is used as a gate electrode material, after patterning the gate electrode material by a second photomask P15, anodic oxidation can be applied to the surface thereof. In this case, a self-aligning process can be employed, whereby the contact hole of a source and drain can be formed closer to the gate, and the TFT characteristic can be further improved thereby, due to the improved mobility as well as

the reduction in threshold voltage.

Thermal annealing process was again carried out at 600 °C, for 10 to 50 hours. By activating impurities, a source 10, a drain 12 of NTFT and a source 18, a drain 20 of PTFT were manufactured as P^+ type and N^+ type. Channel forming regions 19, 11 are formed as semi-amorphous semiconductors, under gate electrodes 21, 9.

In this way, C/TFT can be manufactured without elevating the temperature not less than 700 °C in every process.

Therefore, it is not necessary to use an expensive material such as quartz for the substrate, and this is a most suitable process for manufacturing the wide-screen liquid crystal display device in accordance with the present invention.

The thermal annealing process was carried out twice in this embodiment, as shown in Fig. 14 (A), (D). However, the annealing process shown in Fig.14(A) may be omitted dependent upon the desired characteristics, and the manufacturing time can be shortened by replacing these two annealing processes with only one annealing process shown in Fig.14(D).

Referring to Fig.14(E), a silicon oxide film 85 was formed as an interlayer insulating film by sputtering as described supra. The silicon oxide film can be formed by LPCVD, photo-CVD, or by atmospheric pressure CVD. The thickness thereof was, for example, 0.2 to 0.6μm. Thereafter, an opening 86 for electrode was formed using a photomask P17. Aluminum was then sputtered on the surface of the entire structure, as shown in Fig.14(F), and after a lead 71 as well as a contact 72 was manufactured using a photomask P18, an organic resin 69 for flattening, for example, a translucent polyimide resin was applied to and formed on the surface thereof, and an opening for electrode was formed again by a photomask P19.

An ITO (indium tin oxide) was formed by sputtering, so as to

form two TFTs in a complementary structure, and to connect the output terminal thereof to one picture element electrode of the liquid crystal device, as a transparent electrode. It was then etched using a photomask P20, and an electrode 17 was formed thereby. The ITO was formed at a temperature ranging from room temperature to 150 °C and then annealed at 200 to 400°C in oxygen or atmosphere. The electric characteristics of the TFT thereby obtained were: mobility of 20(cm^2/Vsec), Vth of -5.9(V) for PTFT: and mobility of 40(cm^2/vsec), and Vth of 5.0(V) for NTFT.

In this manner, one substrate for the liquid crystal device was manufactured. The arrangement of the electrode, etc., of the liquid crystal display device is shown in Fig.13. NTFT 13 and PTFT 22 were provided on the intersection of a first signal line 3 and a second signal line 4, whereby the device has a matrix form using C/TFT. NTFT 13 is connected to the second signal line 4 through the contact of the input terminal of a drain 10, while a gate 9 is connected to the signal line 3 forming a multi-layered wiring. The output terminal of a source 12 is connected to an electrode 17 of the picture element through a contact.

On the other hand, regarding PTFT 22, the input terminal of a drain 20 is connected to the second signal line 4 through a contact, while a gate 21 is connected to the signal line 3, and the output terminal of a source 18, to the picture element electrode 17 through a contact, in the same manner as NTFT. This embodiment is formed by repeating such a structure horizontally and vertically.

An ITO(indium tin oxide) was then formed by sputtering on the soda-lime glass plate on which a silicon oxide film was formed by sputtering at a thickness of 2000Å. The ITO was formed at a temperature ranging from room temperature to 150 °C, and was subjected to the annealing process at 200 to 300 °C in oxygen or atmosphere. A color filter layer was then formed thereon in the

same manner as described in the Preferred Embodiment 1 to obtain a second substrate.

A polyimide precursor was then printed on the substrates by an offset method, and was baked in a non-oxidation atmosphere, e.g. in nitrogen, for an hour, at a temperature of 350 °C. It was then subjected to a known rubbing method, so as to change the surface condition of the polyimide, and a means to allow for a liquid crystal molecule to be oriented in a certain direction at least in the initial stage was provided.

The nematic liquid crystal composition was sandwiched by the first and the second substrates as described above, after fixing the periphery of the first and second substrates by an epoxy adhesive. Since the pitch of the leads on the substrate was as fine as 46μm, connection was made by a COG method. In this embodiment, a gold bump provided on an IC chip was connected by an epoxy silver palladium, and the IC chip and the substrate were buried and fixed by epoxy metamorphic acrylic resin for solidification and the sealing of these. A polarizing plate was then attached to the outside thereof, and a transmission type liquid crystal display device was obtained.

The driving waveform used in this embodiment is shown in Fig.15. In this embodiment, a ramp wave is used as shown in Fig.15. Formation of a ramp wave is easy and it is easy to convert original gradation data into it in the ramp wave. Fig. 16 shows a view finder in accordance with this embodiment and a video camera utilizing the view finder. The video camera comprises the electro-optical device 370 manufactured in the manner described supra and a cold cathode tube 371 having flat emission.

When an analogue gradation display is carried out in a normal mode for the electro-optical device comprising, for example, 49,152 pairs of TFTs of 384 x 128 dots formed into a

50mm square (which is obtained by dividing a substrate of 300 mm square into 36 pieces), the variation in TFTs characteristics is ±10% as a whole, and a gradation display having 16 gradation levels is thus an upper limit, whereas, when a digital gradation display is carried out in accordance with the present invention, it is hardly affected by the variation in TFTs characteristics, and a gradation display having 128 gradation levels is thereby possible, while various and subtle expression of 2,097,152 kinds of colors is achieved in a color display mode.

Preferred Embodiment 3

In this embodiment, a projection type image display device as shown in Fig. 17 will be explained.

In this embodiment, the image projecting part for the projection type image display device was assembled by three electro-optical devices 201. Each of devices 201 has a 640 x 480 dots, and 307,200 picture elements were manufactured in a four-inch diagonal: the size per one picture element was 127μm square.

As the structure of the projection type image display device, the electro-optical devices 201 were installed by dividing into three elementary colors of red, green, and blue: it comprises a red filter 202, a green filter 203, a blue filter 204, a reflecting plate 205, prism mirrors 206, 207, a metal halide light source 208 of 150W, and an optical system 209 for focusing.

The substrate of the electro-optical device in accordance with this embodiment was the same as that manufactured in the manner described in the Preferred Embodiment 2, and has a matrix circuit of C/MOS structure. The liquid crystal material used in this embodiment was of dispersion type or polymer dispersion

type.

A schematic diagram is shown in Fig. 18. A mixture comprising a fumaric acid polymer resin and a nematic liquid crystal at a ratio of 65 :35 mixed in a common solvent of xylene was formed on the substrate 210 at a thickness of 10μm by a die-cast method. Then, the solvent was removed in nitrogen atmosphere at a temperature of 120 °C, for 180 minutes, and a liquid crystal dispersion layer 211 was formed thereby. Conduct time can be shortened by reducing the pressure slightly lower than atmosphere.

An ITO(indium tin oxide film) was formed by sputtering. so as to obtain a counter electrode 212. The ITO was formed at a temperature ranging from room temperature to 150 °C. A translucent silicon resin was applied thereon at a thickness of 30μm, by printing, and was baked for thirty minutes at 100 °C. so as to obtain the electro-optical device.

The driving IC used in this embodiment is shown in Fig. 19. The structure of the information electrode side is the same as described in the Preferred Embodiment 1. In a driving circuit 400 connected to the wirings 406, 407 on scanning side, the ramp wave transmitted from a ramp wave oscillating circuit 405 is controlled by flip flop circuits 403, 404 of a clock CLK 408, and a select signal is added thereto.

A gradation display is possible by digitally controlling the timing for cutting the ramp wave on the side of a scanning line by a bipolar pulse on the side of an information line.

For example, when a gradation display is performed in a normal analogue mode for the electro-optical device comprising 307,200 pairs of TFTs of 640 x 480 dots formed in 300mm square, 16 gradation levels are an upper limit due to the variation in TFT characteristics of approximately ±10%. In the case of digital gradation display in accordance with the present invention,

however, since it is hardly affected by the variation in characteristics of TFT devices, a gradation display having 256 gradation levels is possible, while a various and subtle display of as many as 16,777,216 kinds of colors is possible.

The electro-optical device can be applied not only to a front type projection television as illustrated in Fig.17, but also to a rear type projection television.

Preferred Embodiment 4

In this embodiment, an electro-optical device for portable computer was manufactured using a reflection type liquid crystal dispersion display device as shown in Fig.20, and the explanation thereof will be herein made:

The first substrate used in this embodiment was the same as that manufactured in the process in accordance with the Preferred Embodiment 1. A nematic liquid crystal and a fumaric acid polymer resin mixed therein 15% of a black pigment at a ratio of 35 : 65 were dissolved in a common solvent of xylene. The solution was applied on the substrate 210, at a thickness of 10μm, by a die-cast method. The solvent was then removed in nitrogen atmosphere at 120 °C, for 180 minutes, and a liquid crystal dispersion layer 211 was formed thereby.

As the black pigment is used therein, black color appears at the time of light scattering or at the time of application of no electric field, while white color is displayed in a transmission state or at the time of application of electric field, whereby a flat display that was difficult for a dispersion type liquid crystal display is possible like that of the letter written on a sheet of paper.

An ITO(indium tin oxide film) was then formed by sputtering, so as to obtain a counter electrode 212. The ITO was formed at a

temperature ranging from room temperature to 150 °C. A white-colored silicon resin was applied thereon at a thickness of 55μm, by printing, and was baked for ninety minutes at a temperature of 100 °C, so as to obtain the electro-optical device.

As a modification of this embodiment, no black pigment was contained in the liquid crystal dispersion layer 211. In this case, the rear surface has to be made black. In this case, white color appears at the time of light scattering, while black color is displayed in a transmission state. A flat display was possible like that of the letter written on a sheet of paper.

Preferred Embodiment 5

In this embodiment, an electro-optical device provided with modified transfer gate TFTs in complementary structure for one picture element was manufactured by anodic oxidation technique, as shown in Fig.21. The manufacture of the TFTs in accordance with this embodiment is basically the same as that in accordance with the first preferred embodiment, and its processes proceed almost in the same manner as shown in Fig.7, however, since the anodic oxidation technique was employed as mentioned above, metallic material was used as a gate electrode material, so as to utilize the anodic oxidation film thereof as a part of an insulating film, whereby manufacturing process was slightly changed.

Referring to Fig.21, PTFT 95 and NTFT 96 are connected to a common gate wiring 107 at gate terminals thereof, and one of source and drain regions of the PTFT and one of source and drain regions of the NTFT are connected together and connected to the other signal line 102. The other one of the source and drain regions of the NTFT are connected to a common picture element electrode 108.

Referring to Figs.22(A) to 22(G), a silicon oxide film as a blocking layer 99 was manufactured on the glass substrate 98, at a thickness of 1000 to 3000Å, by magnetron RF (high frequency) sputtering. The conditions for the process are: 100% oxygen atmosphere, film formation temperature of 15 °C, output of 400 to 800W, and the pressure of 0.5Pa. The film formation rate was 30 to 100 Å/min. using quartz or single crystalline silicon as a target.

A silicon film 97 was formed thereon by LPCVD (low pressure chemical vapor deposition), sputtering, or by plasma CVD.

Referring to Fig.22(A), the silicon film was photo-etched using a first photomask P21, and a region for PTFT was manufactured on the left hand side of the figure, as well as that for NTFT on the right hand side thereof.

A silicon oxide film as a gate insulating film 103 was formed thereon at a thickness of 500 to 2000Å, e.g. at 700Å. The manufacture thereof was carried out under the same conditions employed for the silicon oxide film 99 as a blocking layer.

The alloy of aluminum and silicon was formed thereon as a material for a gate electrode 107, at a thickness of 3000Å to 1.5μm, e.g. at 1μm, by a known sputtering method.

As the material for the gate electrode beside aluminum silicide, molybdenum (Mo), tungsten (W), titan (Ti), tantalum (Ta), chromium (Cr), or an alloy of these material or an alloy of silicon and these material, or a multi-layered film comprising a silicon layer and a layer of these metal can be used.

Further, a silicon oxide film was formed as an insulating film 106, at a thickness of 3000Å to 1μm, or at 8000Å in this embodiment, by sputtering, on the gate electrode material. Then, the insulating film 106 and the gate electrode 107 were subjected to a patterning process using a second photomask P22, and the gate electrode 107 as well as the insulating film 106

were formed as shown in Fig.22(B).

The substrate was then dipped in an AGW electrolytic solution in which propylene glycol was added to a 3% of tartaric acid solution at a ratio of 9:1, while the gate electrode of aluminum silicide was connected to the anode of a power source, and dc power was applied thereto with platinum used as a cathode, Each of the gate electrodes was connected to corresponding gate wiring and all the gate wirings are connected by a terminal in the vicinity of an end part of the substrate and an anodic oxidation film 100 was formed in the vicinity of the side surface of the gate electrode by anodic oxidation, as shown in Fig.22(C).

As the solution used for the anodic oxidation, typically, a strong acid solution such as sulfuric acid, nitric acid, phosphoric acid, or a mixed acid such as tartaric acid or citric acid mixed with ethylene glycol or propylene glycol, can be used. Salt or alkali solution may be mixed thereto, in order to adjust pH of the solution, when required.

The anodic oxidation was carried out as follows: after current was run at the current density of 2.5mA/cm^2 in a constant current mode, for thirty minutes, then five minutes of process in a constant voltage mode followed, so as to form an aluminum oxide film of 2500Å in the vicinity of the side surface of the gate electrode. When the insulating characteristic of the aluminum oxide was measured using a sample manufactured under the same conditions employed for this oxidation process, resistivity was 10^9 ohm·meter, and dielectric strength was 2 x 10^6V/cm.

The observation of the surface of the sample by a scanning electron microscope revealed unevenness on the surface in an approximately 8000 magnifying power mode, however, no fine hole was observed, which means the evidence of a good insulating film.

After an insulating film 103 on the semiconductor was removed by etching as shown in Fig.22(D), boron was ion-implanted

at a dose of 1 to 5 x $10^{15}cm^{-2}$ as an impurity for PTFT, on the entire surface of the substrate. The doping was carried out at a concentration of approximately 10^{19} atoms·cm^{-3}, so as to form a source, drain region of PTFT. In this embodiment, ion doping was carried out after the insulating film on the surface was removed, however, if the conditions for ion-implantation are changed, doping is possible through the insulating film 103 on the semiconductor film.

A photoresist 110 was formed using a third photomask P23 as shown in Fig.22(E), and after a PTFT region was covered therewith, phosphorus was ion-implanted at a dose of 1 to 5 x $10^{15}cm^{-2}$, to the source and drain region for NTFT, so as to obtain a dope concentration of approximately 10^{20}atoms·cm^{-3}. In the ion doping process as described above, the ion-implanting direction was set oblique to the substrate, in order to allow for the impurity to penetrate into a portion of the semiconductor under the anodic oxidation film in the vicinity of the gate electrode, so as to make the end of the source and drain regions 104, 105 almost identical with the end of the gate electrode. Sufficient insulating function is thereby expected for an anodic oxidation film 100 to an electrode wiring to be formed in a following process, and it is thus not necessary to form another insulating film.

Activation process was carried out by irradiating a laser beam to the source and drain regions. Since the activation process was carried out instantaneously, at the time, it is not necessary to consider the diffusion of the metallic material used for the gate electrode, and TFT of high reliability was manufactured.

Aluminum was formed on the entire surface thereof by sputtering, and after an electrode lead 102 was obtained by patterning using a fourth mask P24, the semiconductor which does

not overlap with an electrode 102, an insulating film 106 on the gate electrode 107, and the anodic oxidation film 100 in the vicinity of the side surface of the gate electrode 107 was etched off, and a complete device separation was carried out so as to complete TFT. In this manufacturing method, complementary TFTs were manufactured using four pieces of masks, which is shown in Fig.22(F).

Referring to Fig.22(G), to achieve complementary TFTs, and to connect the output terminal thereof to one picture element electrode of the liquid crystal device as a transparent electrode, an ITO (indium tin oxide film) was formed by sputtering, and was etched using a fifth photomask ⑤ so as to form a picture element electrode 108.

In this way, modified transfer gate TFTs having arrangement and structure as shown in Fig.21(A), (B), (C), were completed. Fig.21(B) is a cross sectional view corresponding to a F-F' cross section shown in Fig.21(A), while Fig.21(C) is a cross sectional view corresponding to an E-E' cross section shown in Fig.21(A). As clearly shown in Fig.21(B), (C), the interlayer insulating film 106 invariably exists on the gate electrode 107, and it works sufficiently as an interlayer insulating means at an intersection of the lead part of a gate wiring 107 and that of a source or drain wiring 102, whereby the generation of wiring capacity at the intersection was able to be suppressed.

In this embodiment, complementary TFTs having structure in which the capacity in the vicinity of wirings is less, and the fear of short-circuit in the vicinity of the gate insulating film is less could be formed using masks fewer than those used in the first preferred embodiment, without employing a higher-grade process technique such as an anisotropic etching to provide an active element substrate.

The substrate formed in the manner described above was used

as a first substrate and a second substrate (counter substrate) was formed by forming a counter electrode on a substrate and further forming an orientation control film thereon. The first and second substrates were joined with each other and an STN type liquid crystal was injected between the first and second substrate by a known technique. An active matrix type STN liquid crystal electro-optical device was then completed.

The applications to the electro-optical device were described in the above examples, however, the present invention is not limited thereto and the application to other devices or to a three-dimensional integrated circuit device, and so on, is also possible.

The manufacture of TFT device was possible in this embodiment, using masks much fewer than those used in the conventional method. By applying the device of this structure to the manufacture of a semiconductor appliance, as the number of mask was reduced, a manufacturing process was simplified and a production yield was improved, whereby a semiconductor application device was offered at a more inexpensive manufacturing cost.

In this embodiment, the anodic oxidation film was formed on the surface of the metal gate electrode by the anodic oxidation and a three-dimensional wiring having a grade separation was provided thereon which was used for a gate electrode material, and which was provided on the surface thereof. Also, by exposing the contact part alone of a source and drain from the gate electrode and the anodic oxidation film, a feeding point is made closer to the channel and thereby the deterioration in the frequency characteristic of the device, and the increase in ON resistance were prevented.

In the case aluminum was used as a gate electrode material, as in this embodiment, H_2 in the gate oxidation film was reduced

into H by the catalytic effect of aluminum, at the time of annealing process during device formation, and an interfacial level density (Q_{ss}) was reduced much compared with the case a silicon gate was used instead, and a device characteristic was thereby improved.

Since source and drain regions of TFT were self-aligned, and the contact part of the electrode led to the source and drain regions was also positioned in a self-aligning manner, the area of the device required for TFT was reduced, and the circuit integration was improved thereby. When TFT was used as an active device of the electro-optical device, the aperture ratio of liquid crystal panel was increased.

The anodic oxidation film in the vicinity of the side surface of the gate electrode was positively used, and TFT of characterized structure was offered thereby, and the manufacture of TFT could be carried out using the fewest possible masks of at least two pieces.

The foregoing description of preferred embodiments has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form described, and obviously many modifications and variations are possible in light of the above teaching. The embodiments were chosen in order to explain most clearly the principles of the invention and its practical application thereby to enable others in the art to utilize most effectively the invention in various embodiments and with various modifications as are suited to the particular use contemplated. Examples of such modifications are as follows.

The present invention can be applied to an electro-optical device having a circuit shown in Fig.23. The circuit is the same as that shown in Fig.4 except that a capacitor is provided on the substrate and connected to each pixel in parallel with the liquid

crystal of the corresponding pixel as shown in Fig.83.

A nematic liquid crystal, a cholesteric liquid crystal, a ferroelectric liquid crystal or an anti-ferroelectric liquid crystal can be used for a liquid crystal layer provided between a pair of substrates in an electro-optical device of the present invention.

WHAT IS CLAIMED IS:

1. A device having at least one liquid crystal panel, said liquid crystal panel comprising:

a substrate having an insulating surface;

at least one thin film transistor formed over said substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region, and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

an organic rein film formed over said substrate to provide a leveled upper surface over said substrate, said organic resin film covering said thin film transistor; and

a pixel electrode formed over said organic resin film, said pixel electrode being electrically connected to said thin film transistor through an opening formed in said organic resin film,

wherein said channel region comprises crystal silicon and exhibits a peak of Raman spectra displaced from 522 cm^{-1} to the low frequency direction. (Device + Raman shift)

2. A device having at least one liquid crystal panel, said liquid crystal panel comprising:

a substrate having an insulating surface;

at least one thin film transistor formed over said substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film

adjacent to said channel region, and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

an organic rein film formed over said substrate to provide a leveled upper surface over said substrate, said organic resin film covering said thin film transistor; and

a pixel electrode formed over said organic resin film, said pixel electrode being electrically connected to said thin film transistor through an opening formed in said organic resin film,

wherein said channel region comprises crystal silicon and exhibits a peak of Raman spectra displaced from 522 cm^{-1} to the low frequency direction and said channel region contains boron at a concentration of 1 x 10^{15} to 1 x 10^{18} atoms/cm^3. (1 + boron concentration)

3. A device having at least one liquid crystal panel, said liquid crystal panel comprising:

a substrate having an insulating surface;

at least one thin film transistor formed over said substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region, and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

an organic rein film formed over said substrate to provide a leveled upper surface over said substrate, said organic resin film covering said thin film transistor; and

a pixel electrode formed over said organic resin film, said pixel electrode being electrically connected to said thin film transistor through an opening formed in said organic resin film,

wherein said channel region comprises crystal silicon and exhibits a peak of Raman spectra displaced from 522 cm^{-1} to the low frequency direction and said channel region contains oxygen at a concentration not higher than 7 x 10^{19} atoms/cm^3. (1 + oxygen concentration, support for oxygen concentration is page 20, line 19)

4. A device having at least one liquid crystal panel, said liquid crystal panel comprising:

a substrate having an insulating surface;

at least one thin film transistor formed over said substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region, and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

an interlayer insulating film covering said thin film transistor;

a lead electrode comprising aluminum formed on said interlayer insulating film and electrically connected to one of the source or drain regions of said thin film transistor through a hole of said interlayer insulating film;

an organic rein film formed over thin film transistor, said interlayer insulating film and said lead electrode to provide a leveled upper surface; and

a pixel electrode formed over said organic resin film, said pixel electrode being electrically connected to said thin film transistor via said lead electrode,

wherein said channel region comprises crystal silicon and exhibits a peak of Raman spectra displaced from 522 cm^{-1} to the low frequency direction. (1 + lead electrode comprising aluminum)

5. A device having at least one liquid crystal panel, said liquid crystal panel comprising:

a substrate having an insulating surface;

at least one thin film transistor formed over said substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region, and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

an organic rein film formed over said substrate to provide a leveled upper surface over said substrate, said organic resin film covering said thin film transistor; and

a pixel electrode formed over said organic resin film, said pixel electrode being electrically connected to said thin film transistor through an opening formed in said organic resin film,

wherein said channel region comprises crystal silicon of which apparent grain diameter calculated based on half-width of Raman spectra is 50 to 500Å. (1 + Raman grain size)

6. A television comprising:

a tuner for receiving television radio wave;

a liquid crystal panel operationally connected to said tuner, said liquid crystal panel comprising:

a substrate having an insulating surface;

at least one thin film transistor formed over said substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region, and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

an organic rein film formed over said substrate to provide a leveled upper surface over said substrate, said organic resin film covering said thin film transistor; and

a pixel electrode formed over said organic resin film, said pixel electrode being electrically connected to said thin film transistor through an opening formed in said organic resin film,

wherein said channel region comprises crystal silicon and exhibits a peak of Raman spectra displaced from 522 cm^{-1} to the low frequency direction. (TV + Raman shift)

7. A television comprising:

a tuner for receiving television radio wave;

a liquid crystal panel operationally connected to said tuner, said liquid crystal panel comprising:

a substrate having an insulating surface;

at least one thin film transistor formed over said substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region, and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

an organic rein film formed over said substrate to provide a leveled upper surface over said substrate, said organic resin film covering said thin film transistor; and

a pixel electrode formed over said organic resin film, said pixel electrode being electrically connected to said thin film transistor through an opening formed in said organic resin film,

wherein said channel region comprises crystal silicon and exhibits a peak of Raman spectra displaced from 522 cm^{-1} to the low

frequency direction and said channel region contains boron at a concentration of 1 x 10^{15} to 1 x 10^{18} atoms/cm^3. (6 + boron concentration)

8. A television comprising:

a tuner for receiving television radio wave;

a liquid crystal panel operationally connected to said tuner, said liquid crystal panel comprising:

a substrate having an insulating surface;

at least one thin film transistor formed over said substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region, and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

an organic rein film formed over said substrate to provide a leveled upper surface over said substrate, said organic resin film covering said thin film transistor; and

a pixel electrode formed over said organic resin film, said pixel electrode being electrically connected to said thin film transistor through an opening formed in said organic resin film,

wherein said channel region comprises crystal silicon and exhibits a peak of Raman spectra displaced from 522 cm^{-1} to the low frequency direction and said channel region contains oxygen at a concentration not higher than 7 x 10^{19} atoms/cm^3. (6+ oxygen concentration)

9. A television comprising:

a tuner for receiving television radio wave;

a liquid crystal panel operationally connected to said tuner, said liquid crystal panel comprising:

a substrate having an insulating surface;

at least one thin film transistor formed over said substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region, and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

an interlayer insulating film covering said thin film transistor;

a lead electrode comprising aluminum formed on said interlayer insulating film and electrically connected to one of the source or drain regions of said thin film transistor through a hole of said interlayer insulating film;

an organic rein film formed over thin film transistor, said interlayer insulating film and said lead electrode to provide a leveled upper surface; and

a pixel electrode formed over said organic resin film, said pixel electrode being electrically connected to said thin film transistor via said lead electrode,

wherein said channel region comprises crystal silicon and exhibits a peak of Raman spectra displaced from 522 cm^{-1} to the low frequency direction. (6 + lead electrode comprising aluminum)

10. A television comprising:

a tuner for receiving television radio wave;

a liquid crystal panel operationally connected to said tuner, said liquid crystal panel comprising:

a substrate having an insulating surface;

at least one thin film transistor formed over said substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region, and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

an organic rein film formed over said substrate to provide a leveled upper surface over said substrate, said organic resin film covering said thin film transistor; and

a pixel electrode formed over said organic resin film, said pixel electrode being electrically connected to said thin film transistor through an opening formed in said organic resin film,

wherein said channel region comprises crystal silicon of which apparent grain diameter calculated based on half-width of Raman spectra is 50 to 500Å. (6 + Raman grain size)

11. A portable computer having a liquid crystal panel, said liquid crystal panel comprising:

a substrate having an insulating surface;

at least one thin film transistor formed over said substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region, and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

an organic rein film formed over said substrate to provide a leveled upper surface over said substrate, said organic resin film covering said thin film transistor; and

a pixel electrode formed over said organic resin film, said pixel electrode being electrically connected to said thin film transistor through an opening formed in said organic resin film,

wherein said channel region comprises crystal silicon and exhibits a peak of Raman spectra displaced from 522 cm^{-1} to the low frequency direction. (portable computer + Raman shift)

12. A portable computer having a liquid crystal panel, said liquid crystal panel comprising:

a substrate having an insulating surface;

at least one thin film transistor formed over said substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region, and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

an organic rein film formed over said substrate to provide a leveled upper surface over said substrate, said organic resin film covering said thin film transistor; and

a pixel electrode formed over said organic resin film, said pixel electrode being electrically connected to said thin film transistor through an opening formed in said organic resin film,

wherein said channel region comprises crystal silicon and exhibits a peak of Raman spectra displaced from 522 cm^{-1} to the low frequency direction and said channel region contains boron at a concentration of 1×10^{15} to 1×10^{18} atoms/cm^3. (11 + boron concentration)

13. A portable computer having a liquid crystal panel, said liquid crystal panel comprising:

a substrate having an insulating surface;

at least one thin film transistor formed over said substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region, and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

an organic rein film formed over said substrate to provide a leveled upper surface over said substrate, said organic resin film covering said thin film transistor; and

a pixel electrode formed over said organic resin film, said pixel electrode being electrically connected to said thin film transistor through an opening formed in said organic resin film,

wherein said channel region comprises crystal silicon and exhibits a peak of Raman spectra displaced from 522 cm^{-1} to the low frequency direction and said channel region contains oxygen at a concentration not higher than 7 x 10^{19} atoms/cm^3. (11 + oxygen concentration, support for oxygen concentration is page 20, line 19)

14. A portable computer having a liquid crystal panel, said liquid crystal panel comprising:

a substrate having an insulating surface;

at least one thin film transistor formed over said substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region, and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

an interlayer insulating film covering said thin film transistor;

a lead electrode comprising aluminum formed on said interlayer insulating film and electrically connected to one of the source or drain regions of said thin film transistor through a hole of said interlayer insulating film;

an organic rein film formed over thin film transistor, said interlayer insulating film and said lead electrode to provide a leveled upper surface; and

a pixel electrode formed over said organic resin film, said pixel electrode being electrically connected to said thin film transistor via said lead electrode,

wherein said channel region comprises crystal silicon and exhibits a peak of Raman spectra displaced from 522 cm^{-1} to the low frequency direction. (11 + lead electrode comprising aluminum)

15. A portable computer having a liquid crystal panel, said liquid crystal panel comprising:

a substrate having an insulating surface;

at least one thin film transistor formed over said substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region, and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

an organic rein film formed over said substrate to provide a leveled upper surface over said substrate, said organic resin film covering said thin film transistor; and

a pixel electrode formed over said organic resin film, said pixel electrode being electrically connected to said thin film transistor through an opening formed in said organic resin film,

wherein said channel region comprises crystal silicon of which apparent grain diameter calculated based on half-width of Raman spectra is 50 to 500Å. (11 + Raman grain size)

16. A device computer having a liquid crystal panel, said liquid crystal panel comprising:

a first substrate having an insulating surface;

at least one thin film transistor formed over said substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region, and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

an organic rein film formed over said substrate to provide a leveled upper surface over said substrate, said organic resin film covering said thin film transistor;

a pixel electrode formed over said organic resin film, said pixel electrode being electrically connected to said thin film transistor through an opening formed in said organic resin film;

a second substrate opposed to said first substrate with a liquid crystal material interposed therebetween;

a black stripe formed on said second substrate;

an organic leveling film covering said color filter over said second substrate;

a transparent conductive film formed on said organic leveling film; and

an orientation film formed on said transparent conductive film.

17. A television comprising:

a tuner for receiving television radio wave;

a liquid crystal panel operationally connected to said tuner, said liquid crystal panel comprising:

a first substrate having an insulating surface;

at least one thin film transistor formed over said substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region, and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

an organic rein film formed over said substrate to provide a leveled upper surface over said substrate, said organic resin film covering said thin film transistor;

a pixel electrode formed over said organic resin film, said pixel electrode being electrically connected to said thin film transistor through an opening formed in said organic resin film;

a second substrate opposed to said first substrate with a liquid crystal material interposed therebetween;

a black stripe formed on said second substrate;

an organic leveling film covering said color filter over said second substrate;

a transparent conductive film formed on said organic leveling film; and

an orientation film formed on said transparent conductive film.

18. A device having at least one flat panel display, said flat panel display comprising:

a substrate having an insulating surface;

at least one thin film transistor formed over said substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region, and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

an organic rein film formed over said substrate to provide a leveled upper surface over said substrate, said organic resin film covering said thin film transistor; and

a pixel electrode formed over said organic resin film, said pixel electrode being electrically connected to said thin film transistor through an opening formed in said organic resin film,

wherein said channel region comprises crystal silicon and exhibits a peak of Raman spectra displaced from 522 cm^{-1} to the low frequency direction. (1 - LCD)

19. A device having at least one flat panel display, said flat panel display comprising:

a substrate having an insulating surface;

at least one thin film transistor formed over said substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region, and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

an organic rein film formed over said substrate to provide a leveled upper surface over said substrate, said organic resin film covering said thin film transistor; and

a pixel electrode formed over said organic resin film, said pixel electrode being electrically connected to said thin film transistor through an opening formed in said organic resin film,

wherein said channel region comprises crystal silicon and exhibits a peak of Raman spectra displaced from 522 cm^{-1} to the low frequency direction and said channel region contains boron at a concentration of 1 x 10^{15} to 1 x 10^{18} atoms/cm^3. (2- LCD)

20. A device having at least one flat panel display, said flat panel display comprising:

a substrate having an insulating surface;

at least one thin film transistor formed over said substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region, and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

an interlayer insulating film covering said thin film transistor;

a lead electrode comprising aluminum formed on said interlayer insulating film and electrically connected to one of the source or drain regions of said thin film transistor through a hole of said interlayer insulating film;

an organic rein film formed over thin film transistor, said interlayer insulating film and said lead electrode to provide a leveled upper surface; and

a pixel electrode formed over said organic resin film, said pixel electrode being electrically connected to said thin film transistor via said lead electrode,

wherein said channel region comprises crystal silicon and exhibits a peak of Raman spectra displaced from 522 cm^{-1} to the low frequency direction. (4- LCD)

21. A portable computer having at least one flat panel display, said flat panel display comprising:

a substrate having an insulating surface;

at least one thin film transistor formed over said substrate, said thin film transistor including at least a channel region, source and drain regions with said channel region therebetween, a gate insulating film adjacent to said channel region, and a gate electrode adjacent to said channel region with said gate insulating film interposed therebetween;

an organic rein film formed over said substrate to provide a leveled upper surface over said substrate, said organic resin film covering said thin film transistor; and

a pixel electrode formed over said organic resin film, said pixel electrode being electrically connected to said thin film transistor through an opening formed in said organic resin film,

wherein said channel region comprises crystal silicon and exhibits a peak of Raman spectra displaced from 522 cm^{-1} to the low frequency direction and said channel region contains boron at a concentration of 1×10^{15} to 1×10^{18} atoms/cm^3. (12- LCD)

ABSTRACT OF THE DISCLOSURE

A novel structure of an active electro-optical device is disclosed. The device is provided with complementary thin film insulated gate field effect transistors (TFTs) therein which comprise a P-TFT and an N-TFT. P-TFT and N-TFT are connected to a common signal line by the gate electrodes thereof, while the source (or drain) electrodes thereof are connected to a common signal line as well as to one of the picture element electrodes.

In case of driving the active electro-optical device, a gradation display can be carried out in a driving method having a display timing determined in relation to a time F for writing one screen and a time (t) for writing in one picture element, by applying a reference signal in a cycle of the time (t), to the signal line used for a certain picture element driving selection, and by applying the select signal to the other signal line at a certain timing within the time (t), and whereby setting the value of the voltage to be applied to a liquid crystal.

FIG. 1

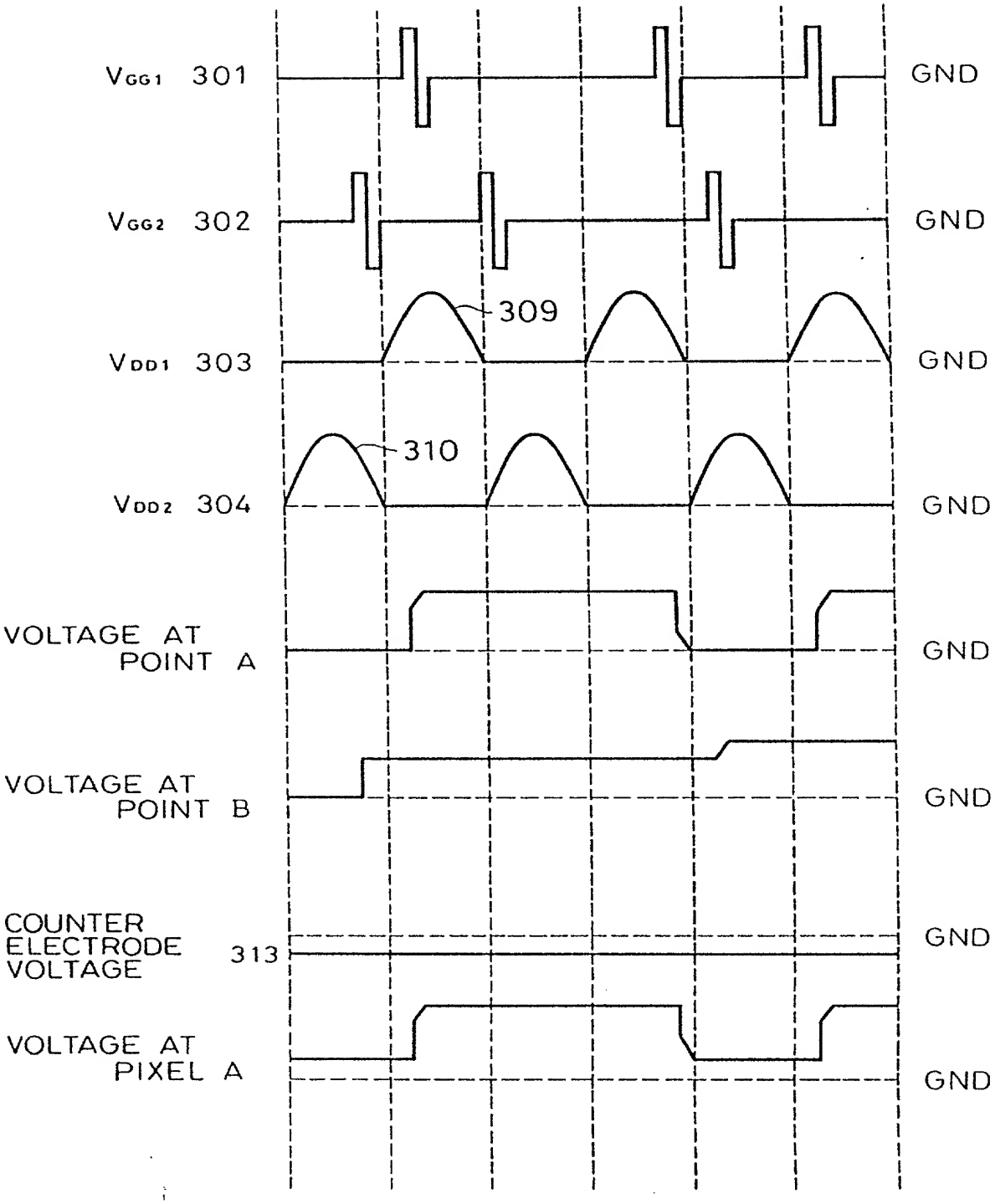

VGG1 301
GND
VGG2 302
GND
309
VDD1 303
GND
310
VDD2 304
GND
VOLTAGE AT POINT A
GND
VOLTAGE AT POINT B
GND
COUNTER ELECTRODE VOLTAGE
313
GND
VOLTAGE AT PIXEL A
GND

FIG. 2

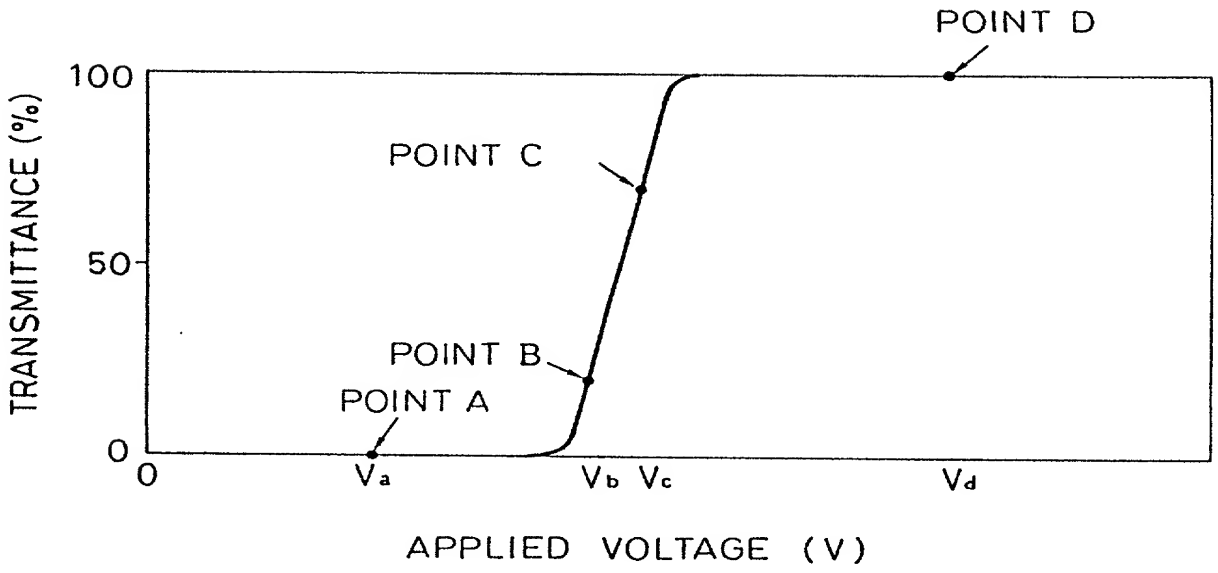

POINT D
100
POINT C
50
POINT B
POINT A
TRANSMITTANCE (%)
0
0
Va
Vb Vc
Vd
APPLIED VOLTAGE (V)

FIG. 3

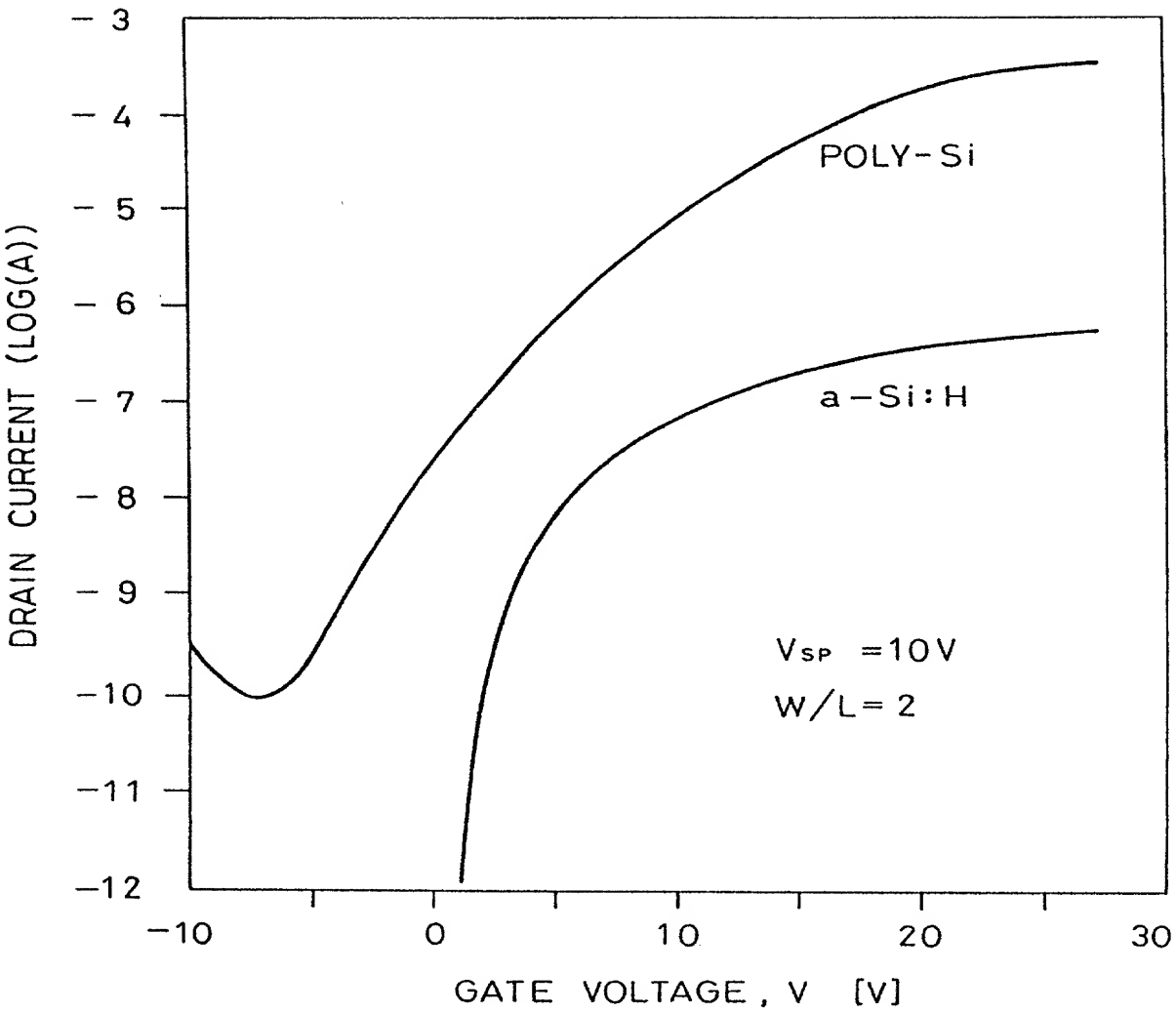

DRAIN CURRENT (LOG(A))
-3
-4
-5
-6
-7
-8
-9
-10
-11
-12
-10
0
10
20
30
GATE VOLTAGE, V [V]
POLY-Si
a-Si:H
VSP =10V
W/L=2

FIG. 4(A)

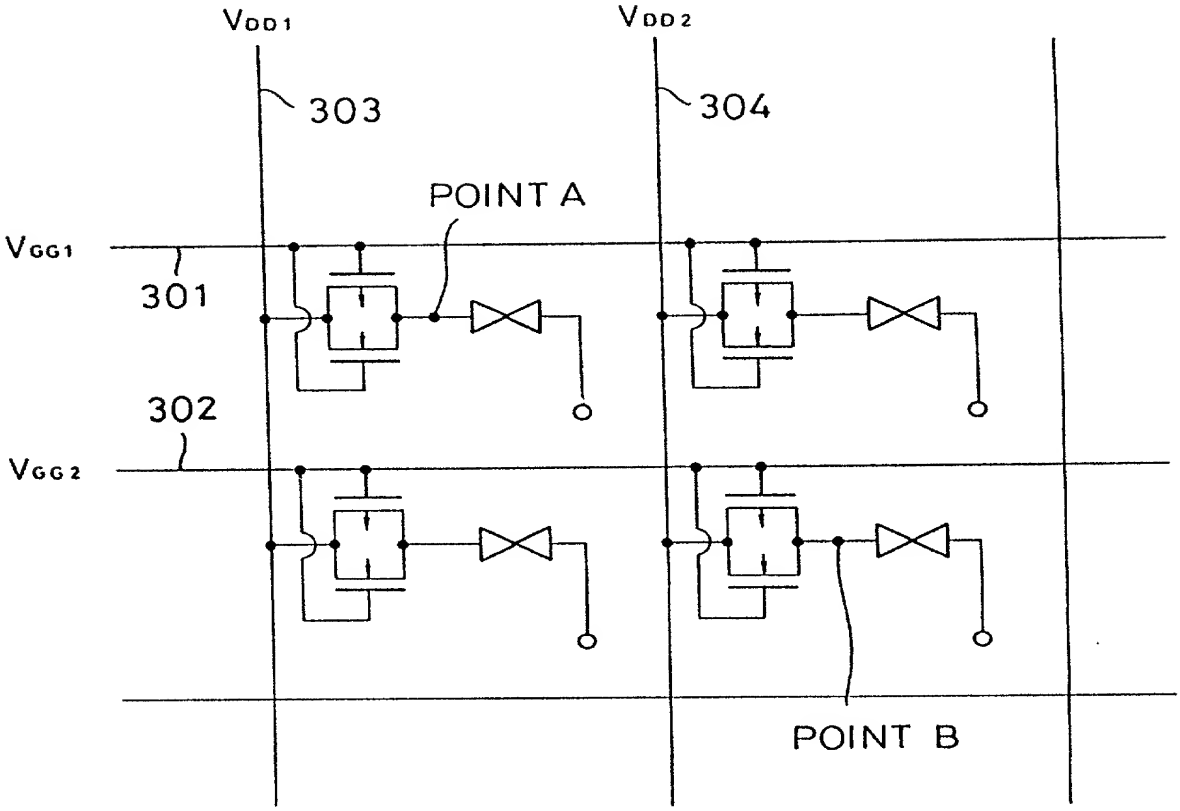


FIG. 4 (B)

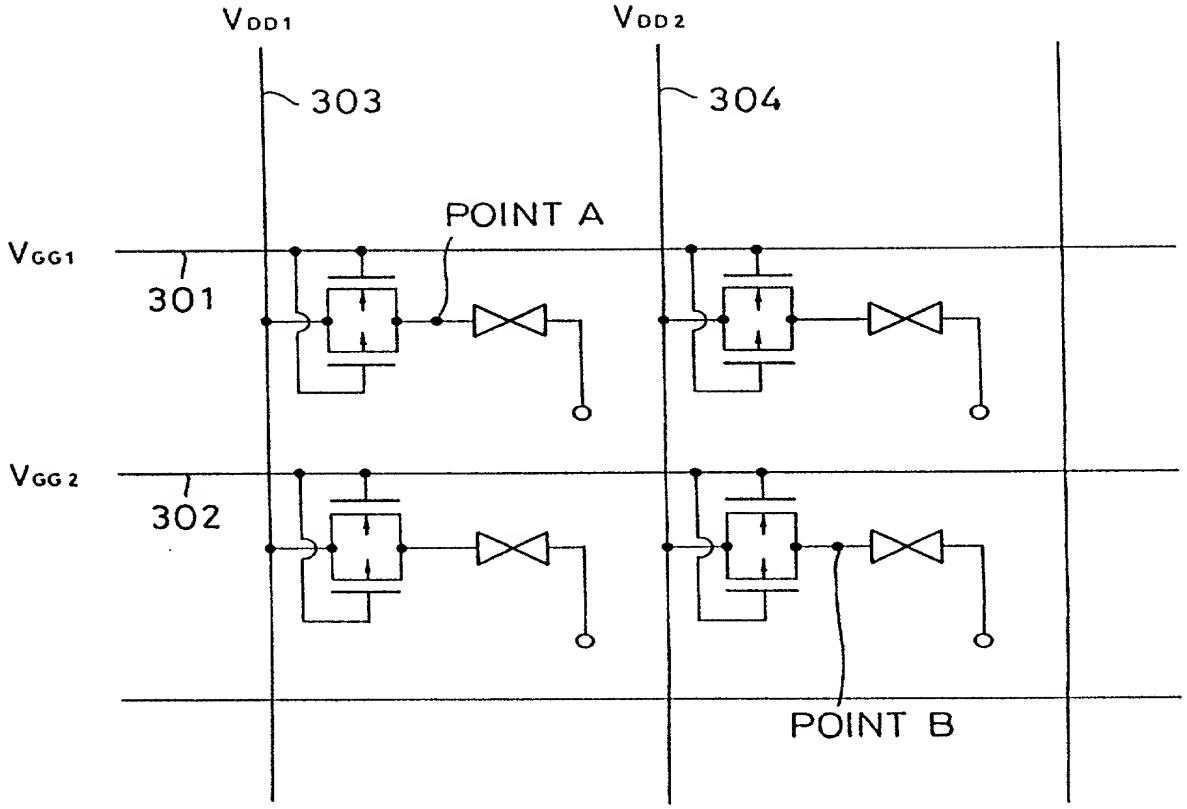


FIG. 5

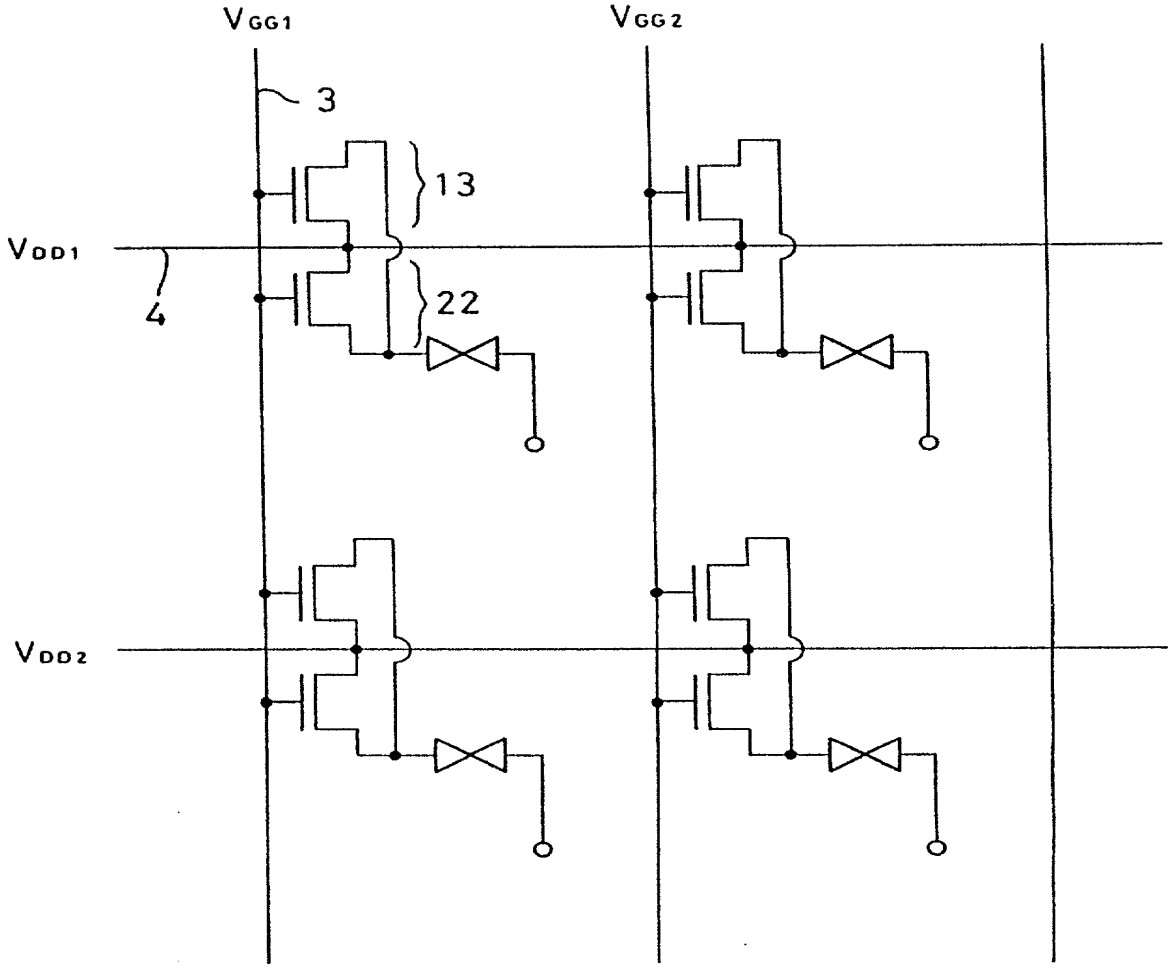


FIG. 6

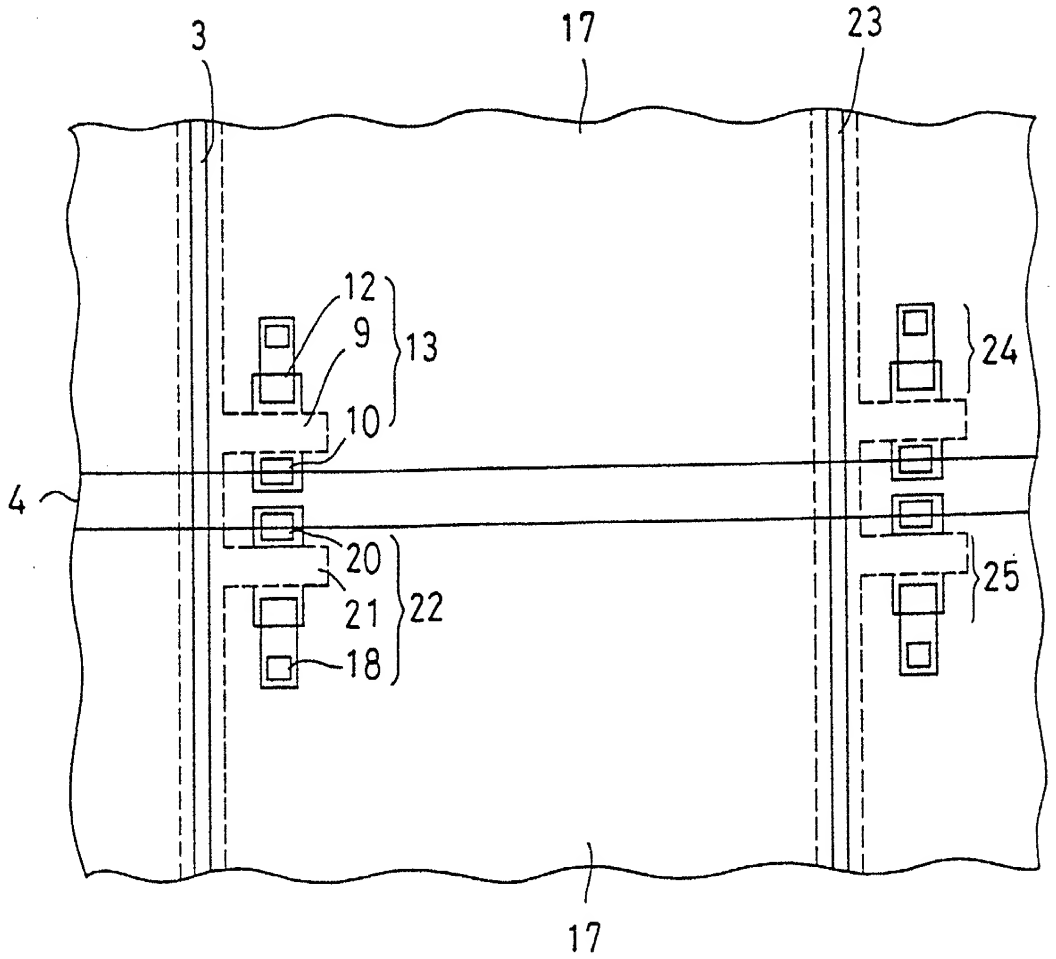


FIG. 7(A)

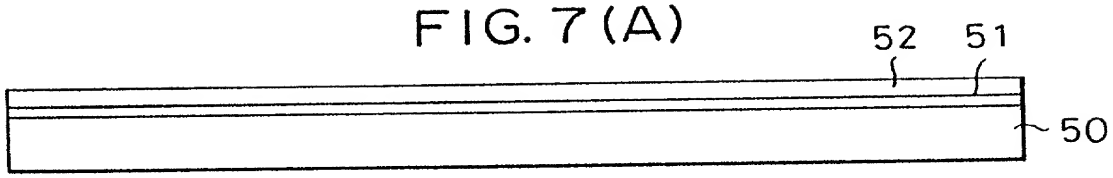


FIG. 7(B)

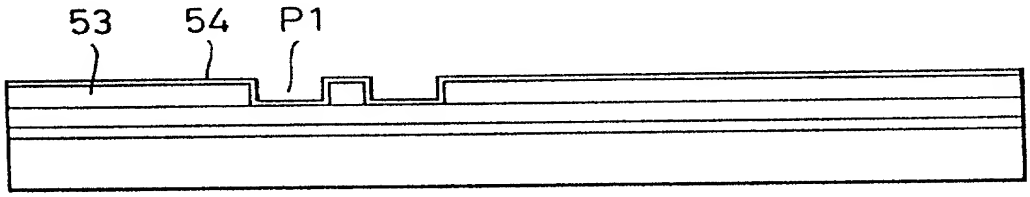


FIG. 7(C)

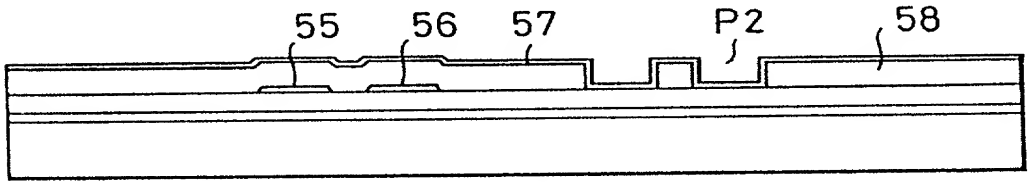


FIG. 7(D)

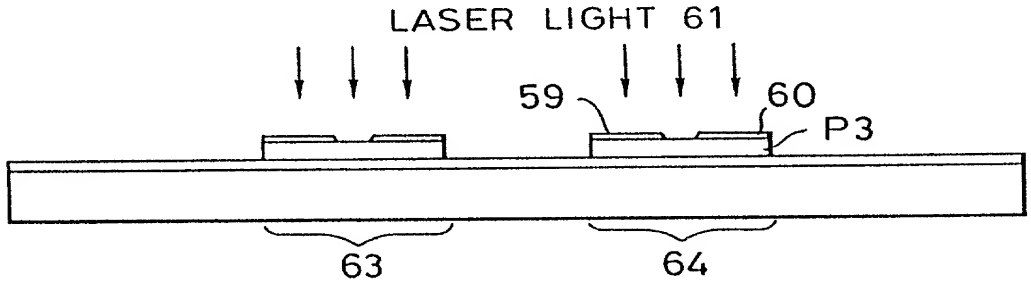


FIG. 7(E)

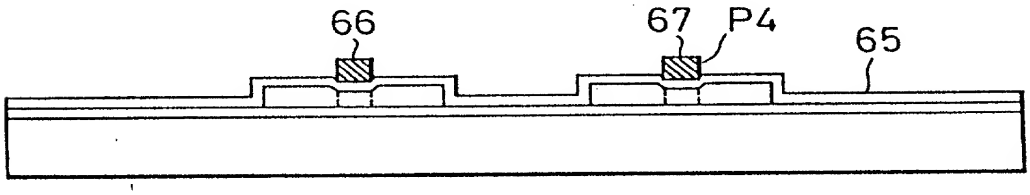


FIG. 7(F)

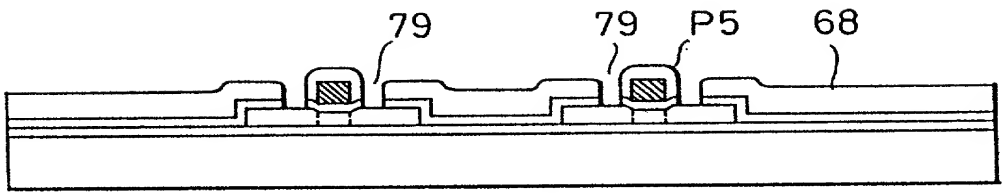


FIG. 7(G)

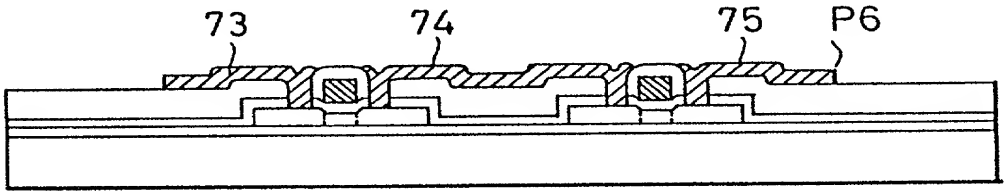


FIG. 7(H)

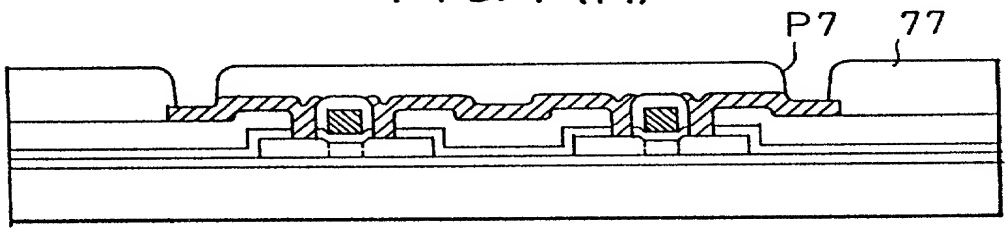


FIG. 7(I)

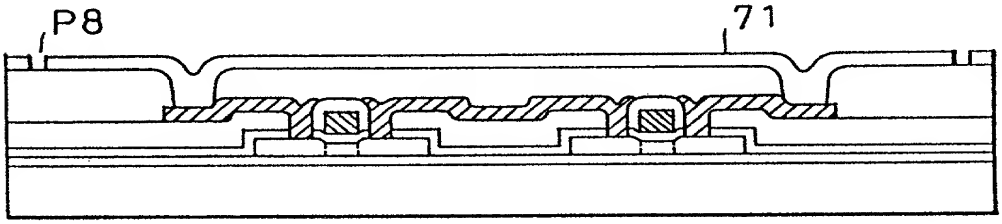


FIG. 8

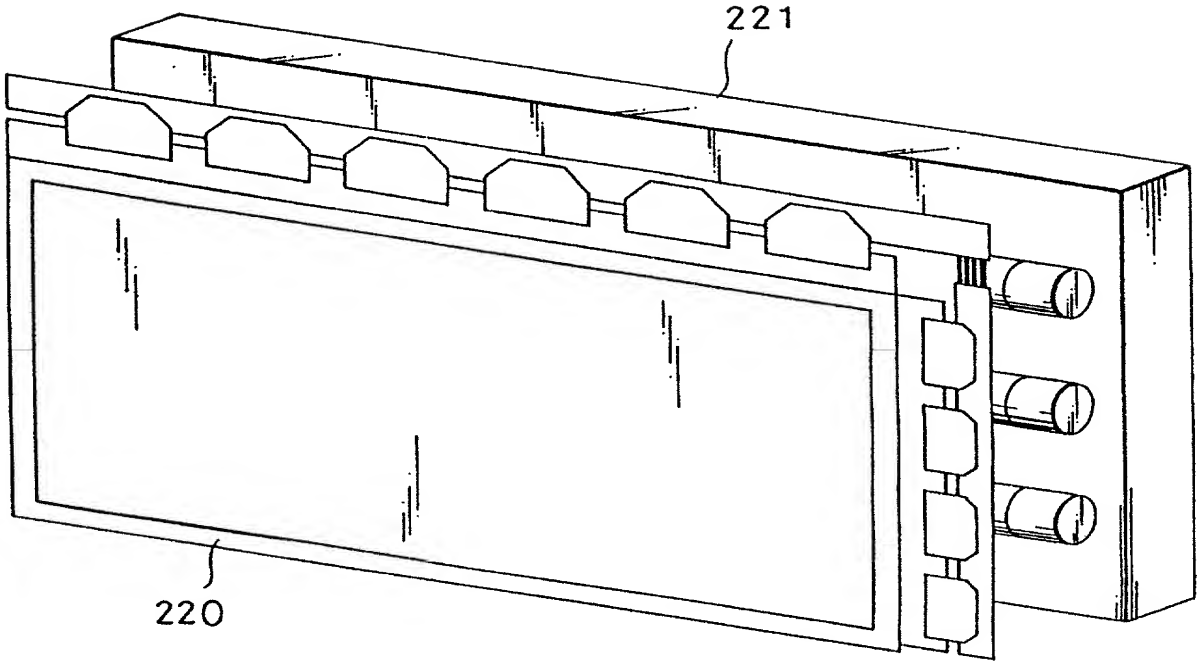


FIG. 9

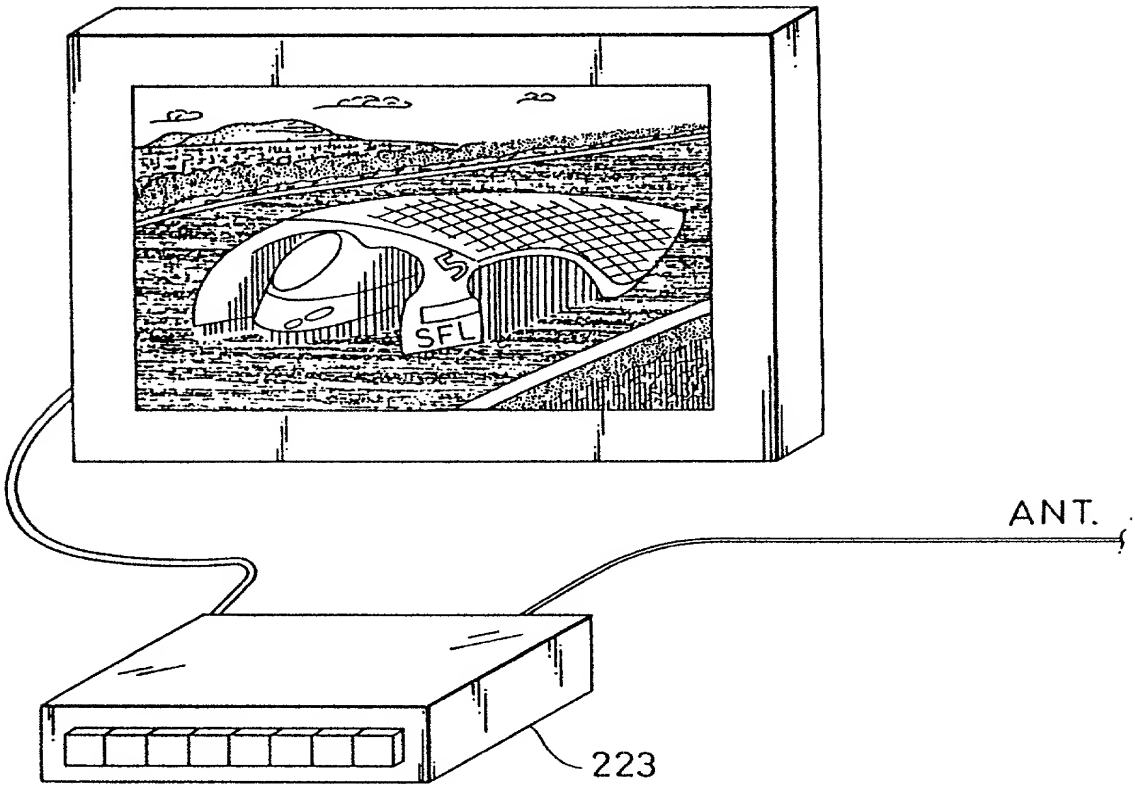


FIG. 10

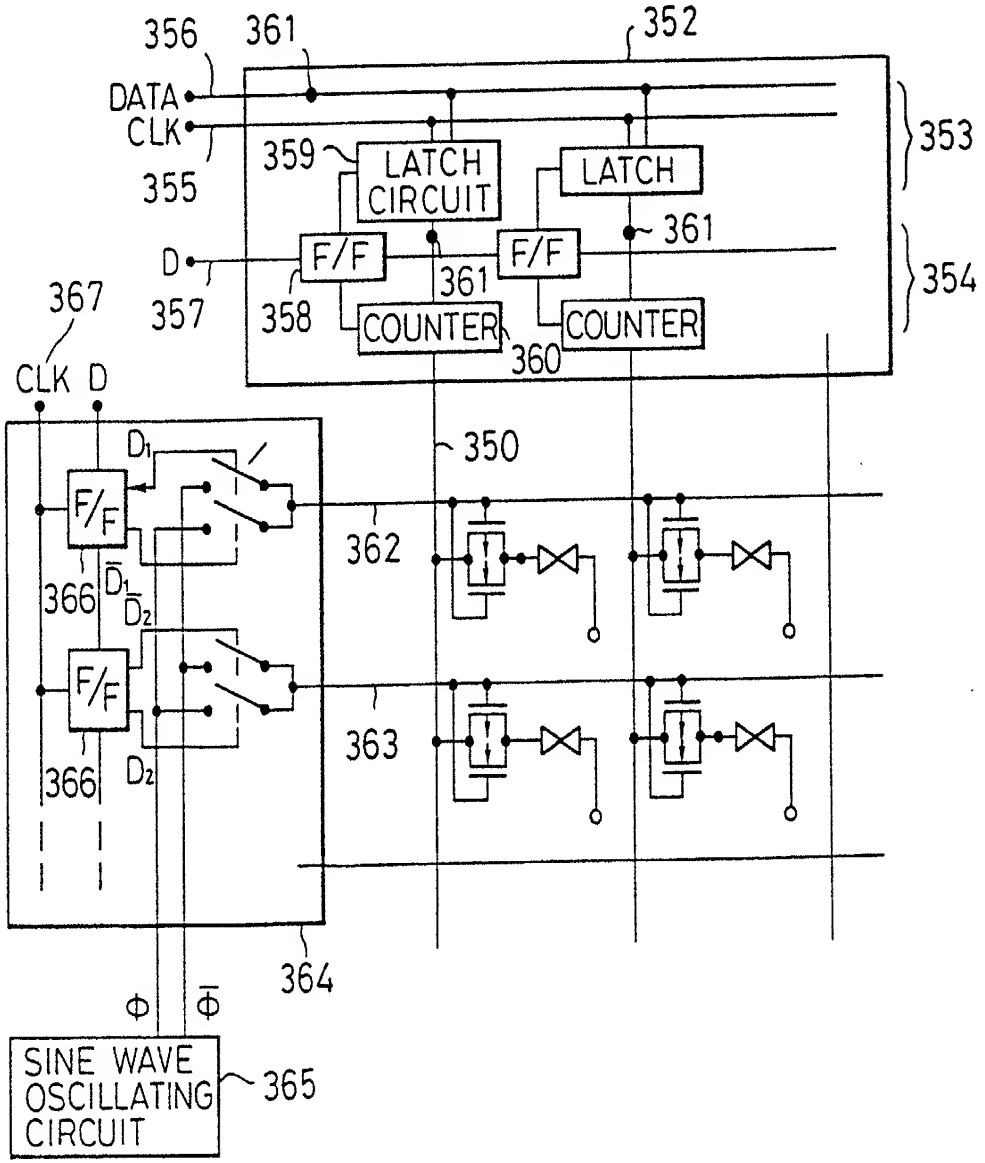


FIG. 11

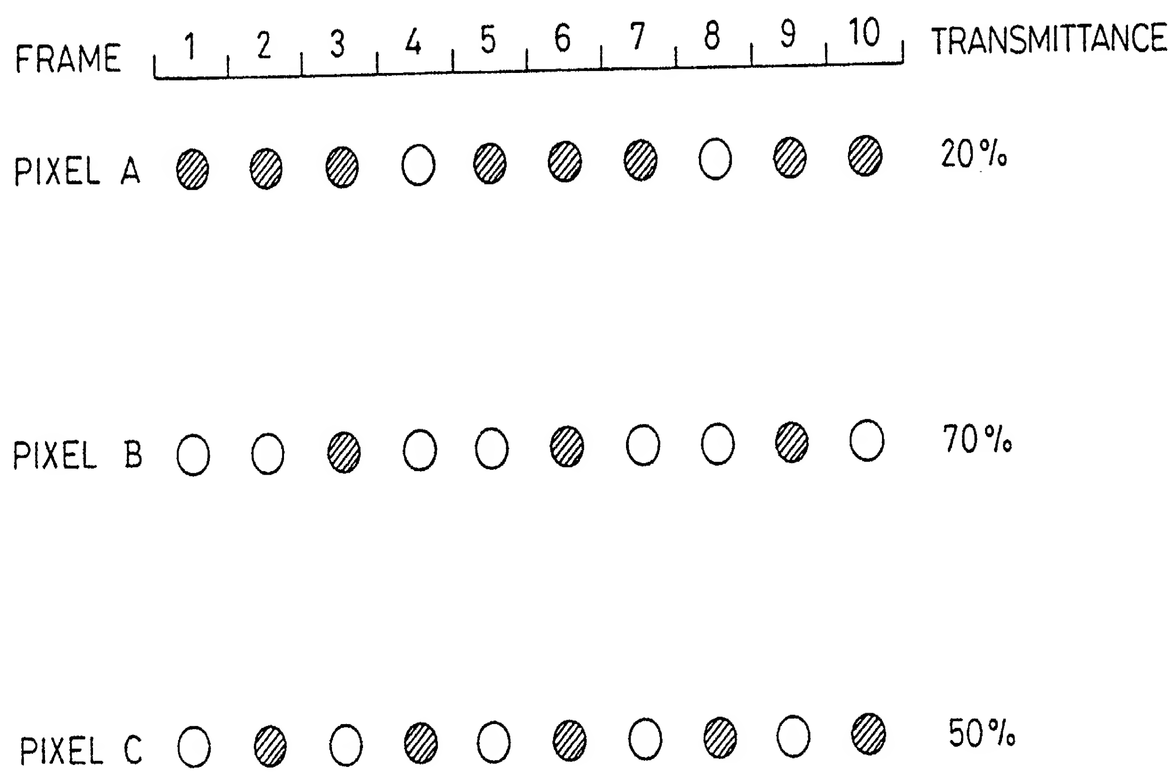

FRAME
1
2
3
4
5
6
7
8
9
10
TRANSMITTANCE
PIXEL A
20%
PIXEL B
70%
PIXEL C
50%

FIG. 12(A)

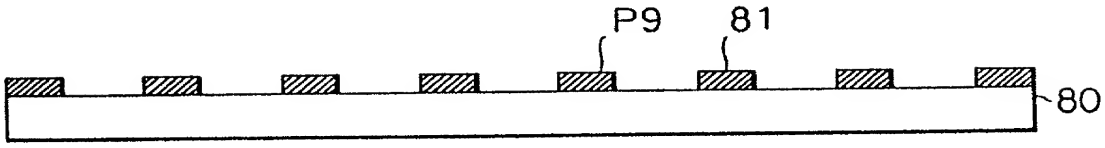


FIG. 12(B)

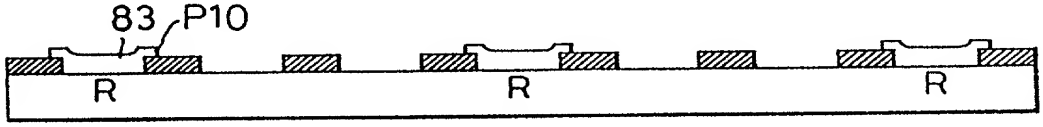


FIG. 12(C)

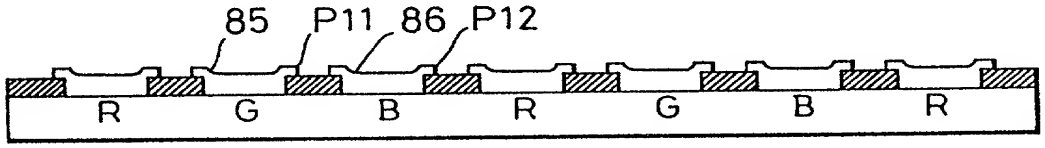


FIG. 12(D)

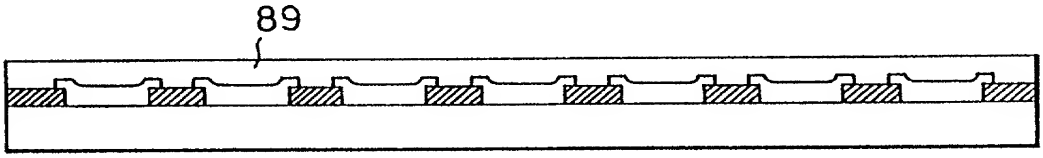


FIG. 12(E)

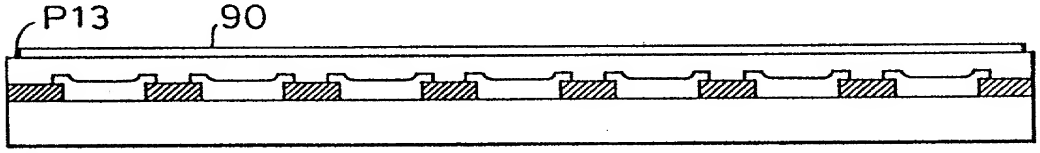
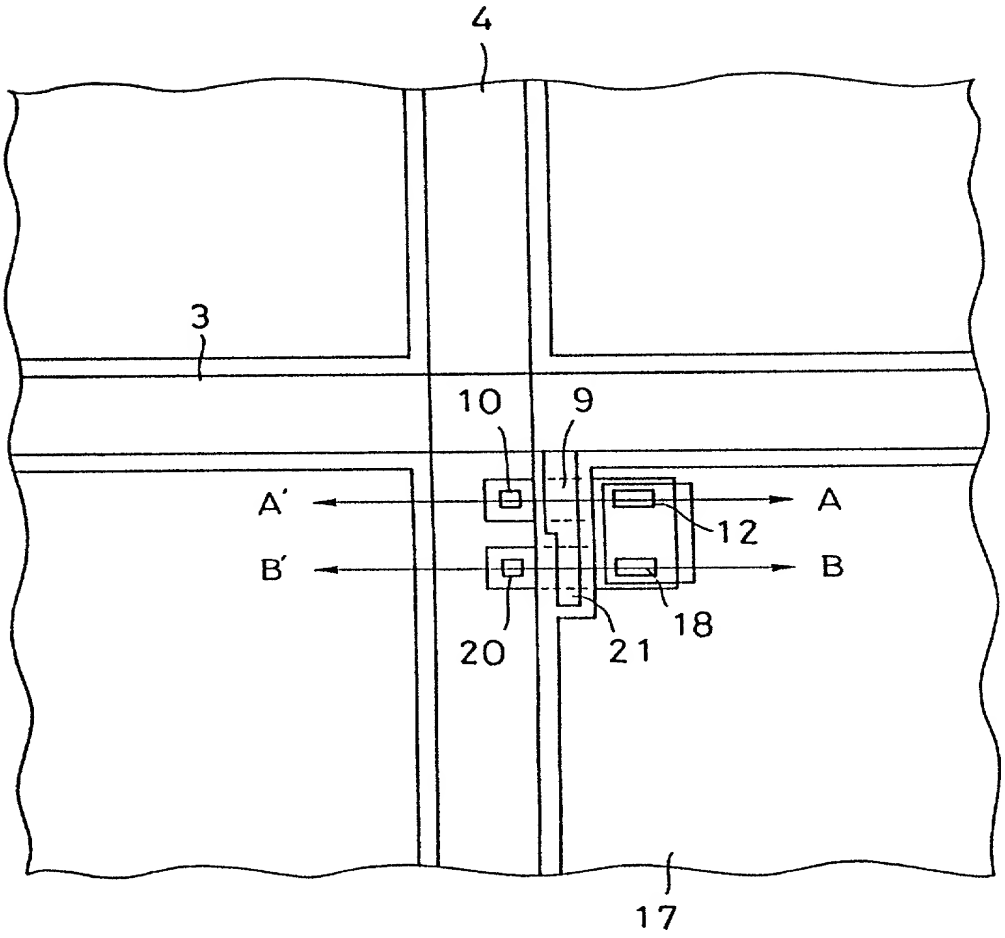


FIG. 13



nTFT
A-A CROSS SECTION

pTFT
B-B CROSS SECTION

FIG. 14 (A)

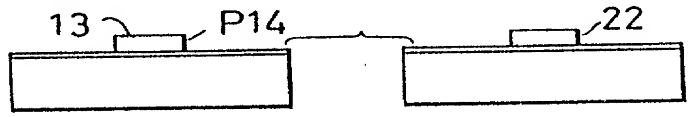


FIG. 14 (B)

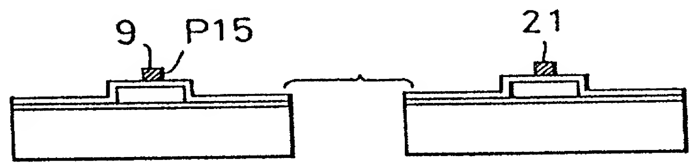


FIG. 14 (C)

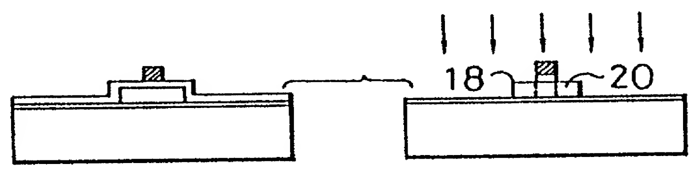


FIG. 14 (D)

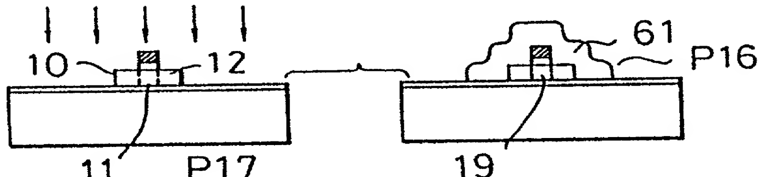


FIG. 14 (E)

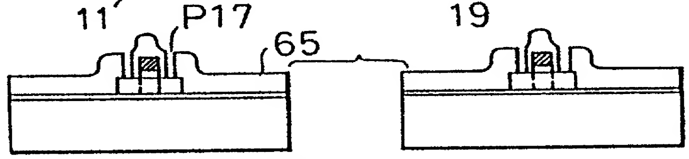


FIG. 14 (F)

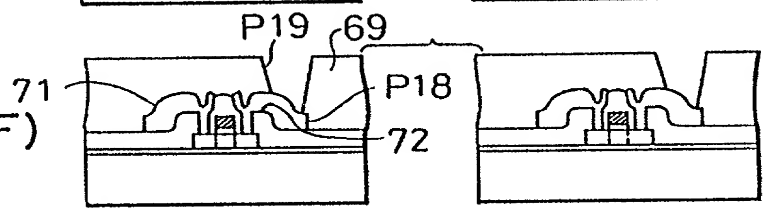


FIG. 14 (G)

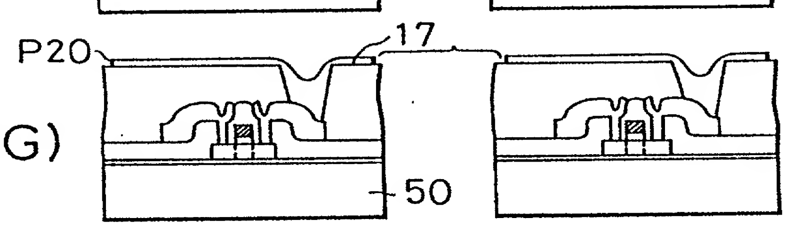


FIG. 15

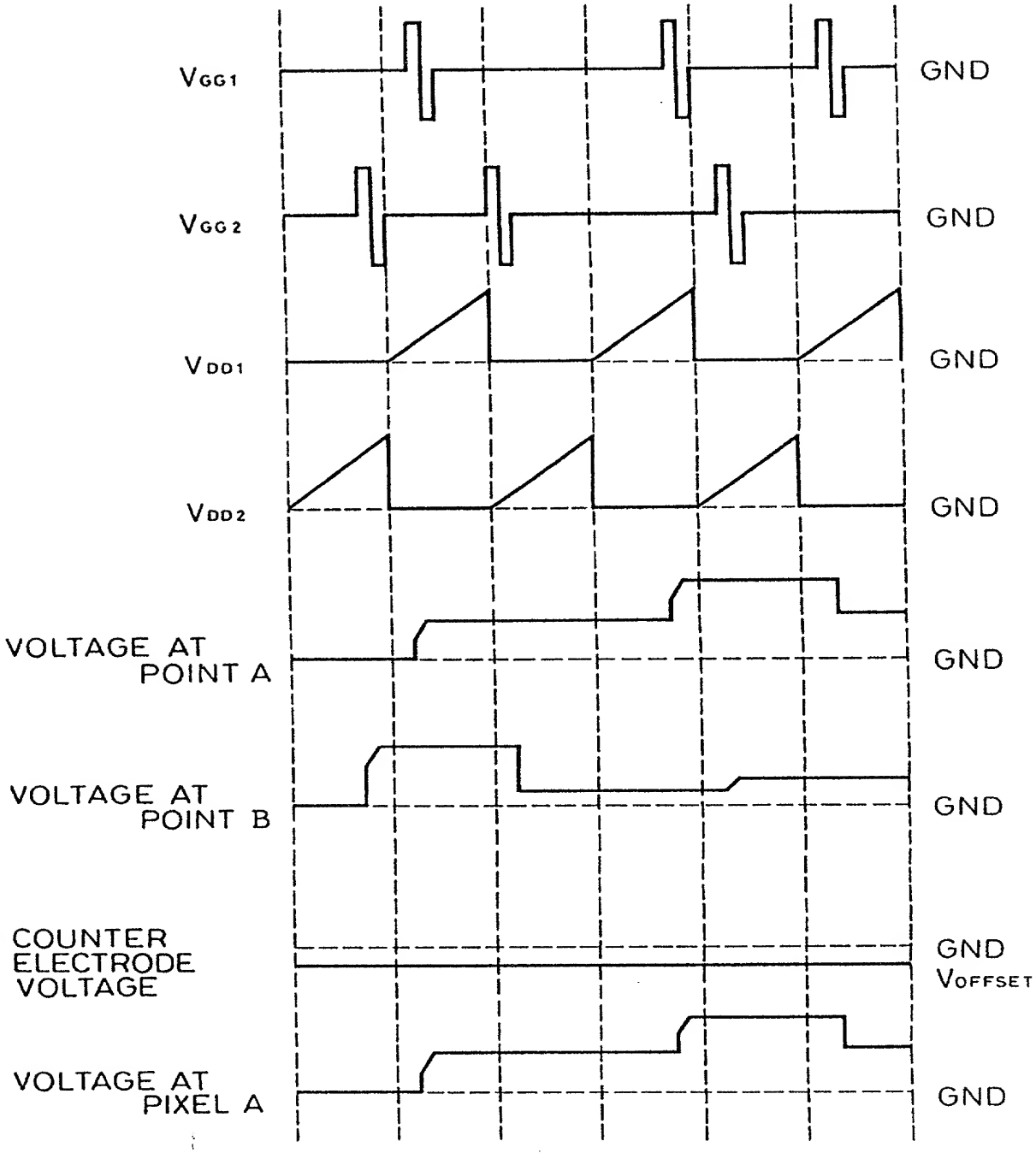

VGG1
GND
VGG2
GND
VDD1
GND
VDD2
GND
VOLTAGE AT POINT A
GND
VOLTAGE AT POINT B
GND
COUNTER ELECTRODE VOLTAGE
GND
VOFFSET
VOLTAGE AT PIXEL A
GND

FIG. 16

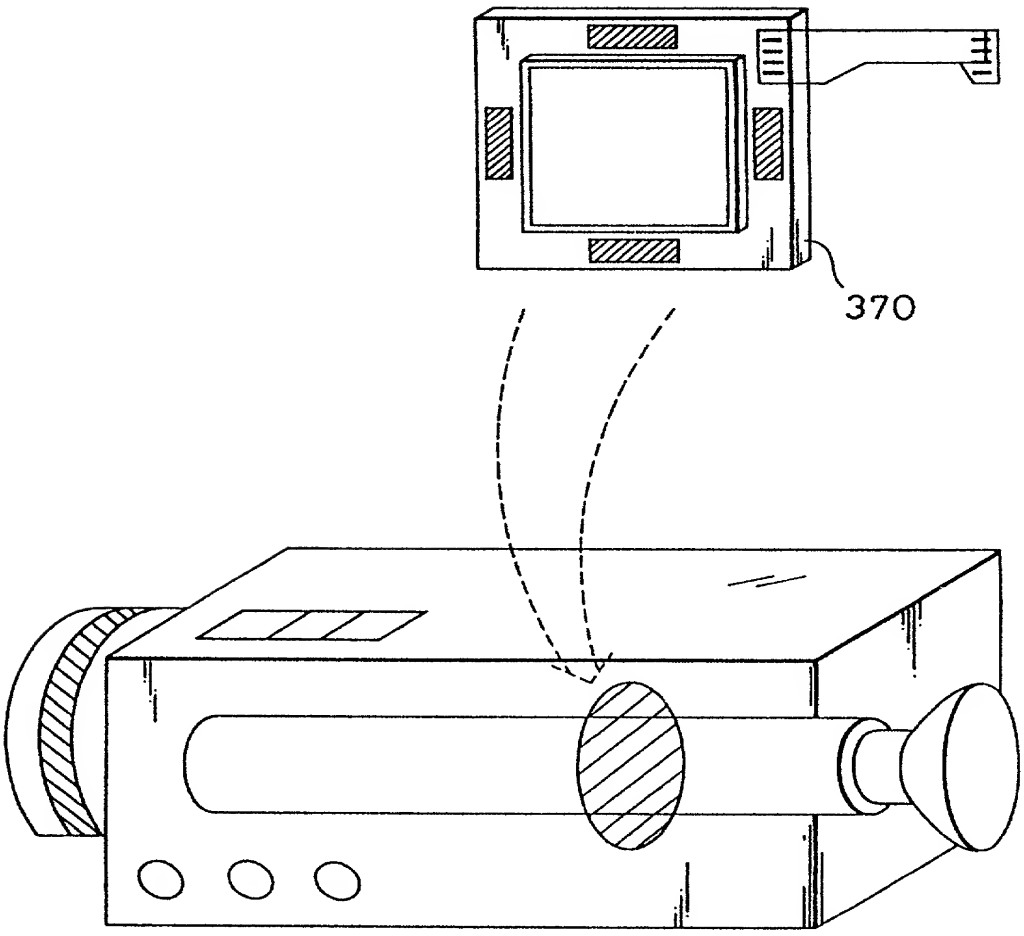


FIG. 17

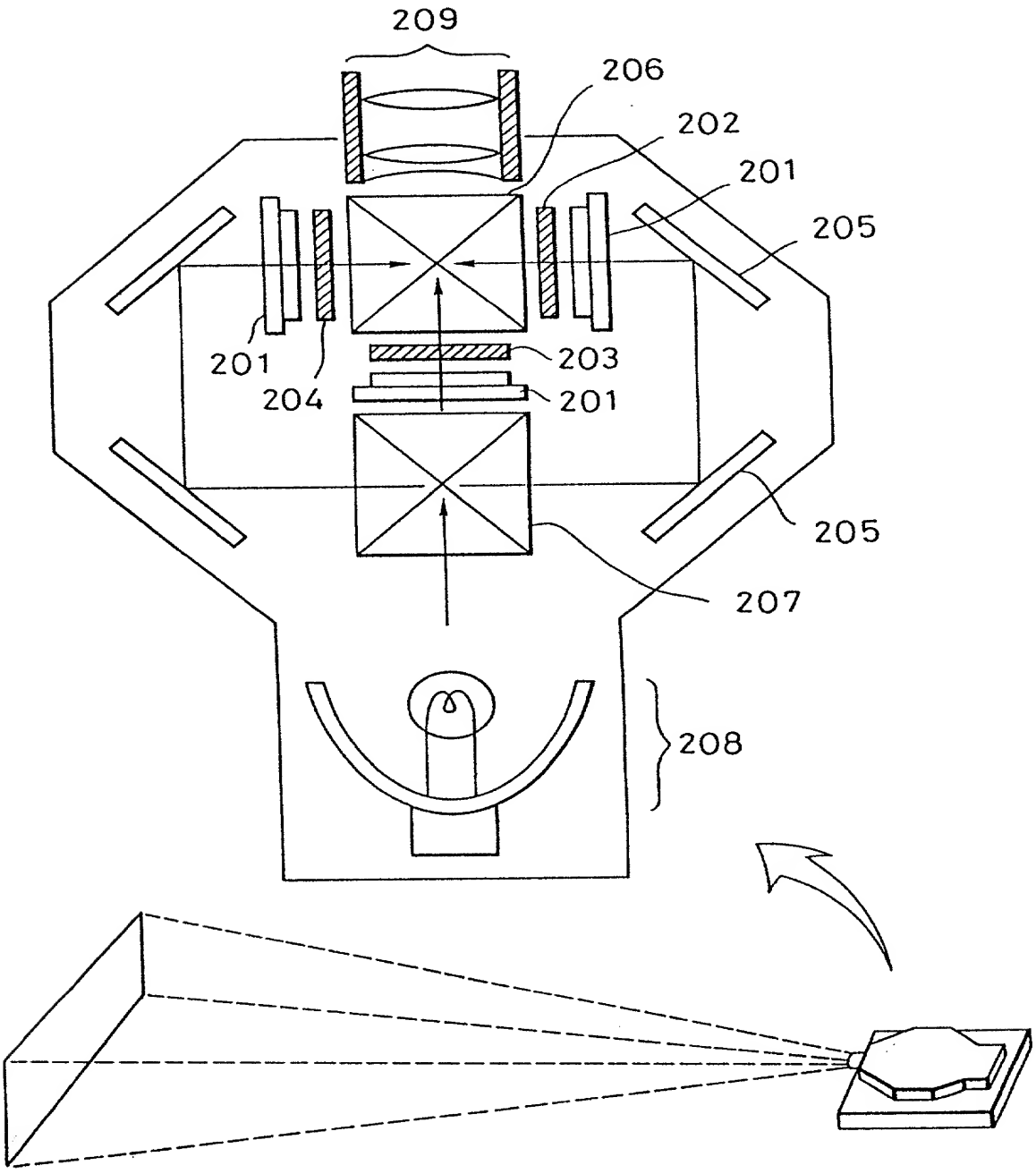


FIG. 18

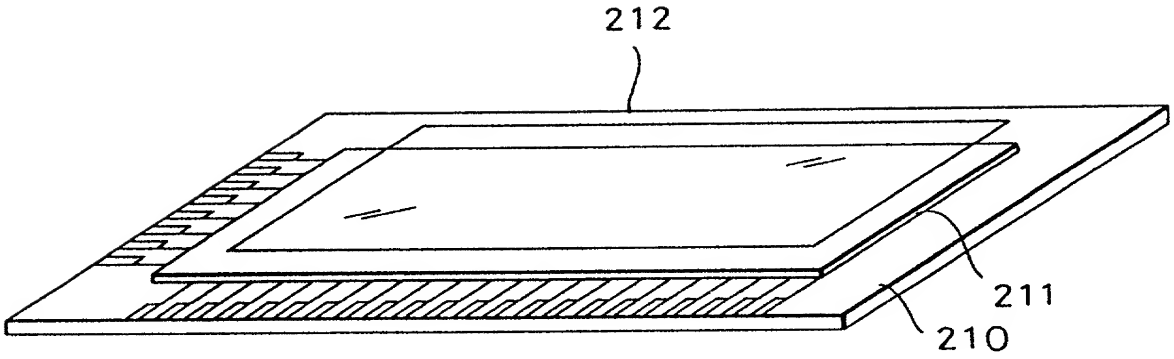


FIG. 19

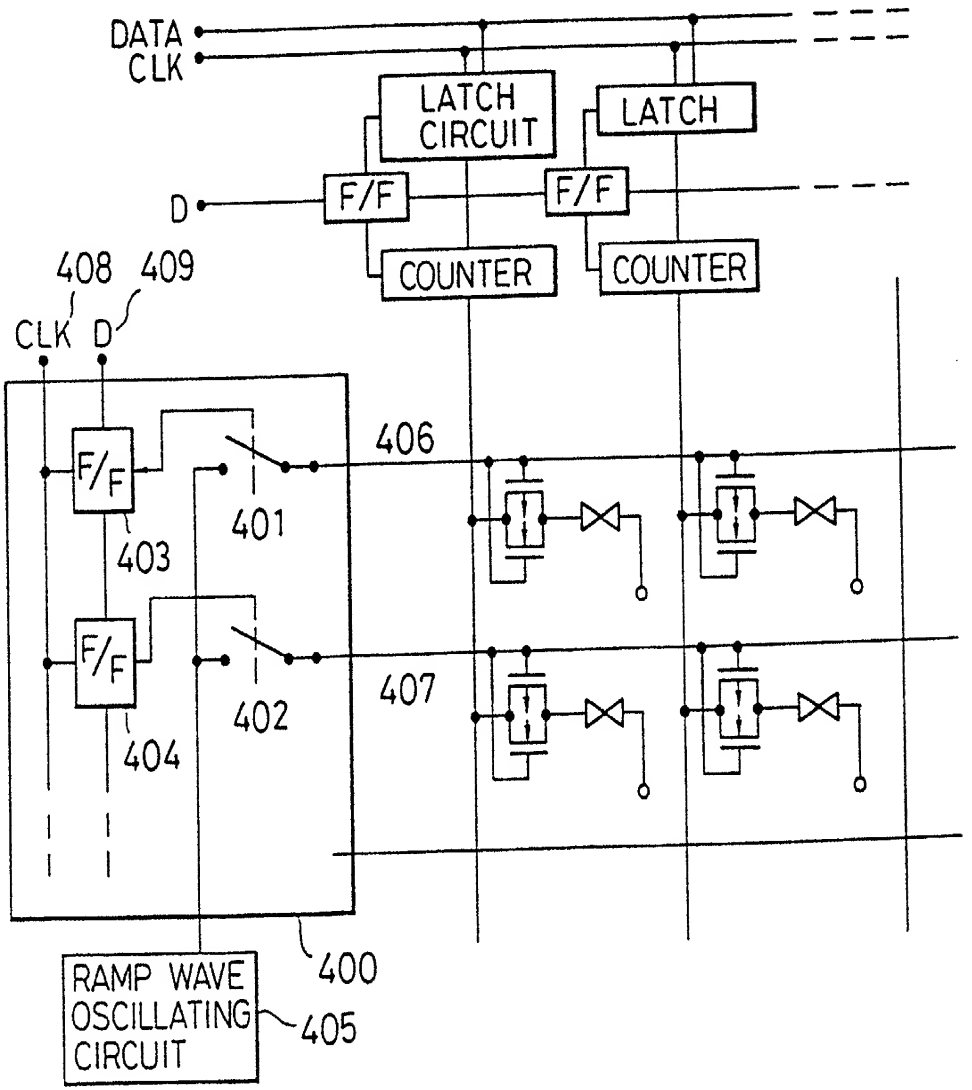


FIG. 20

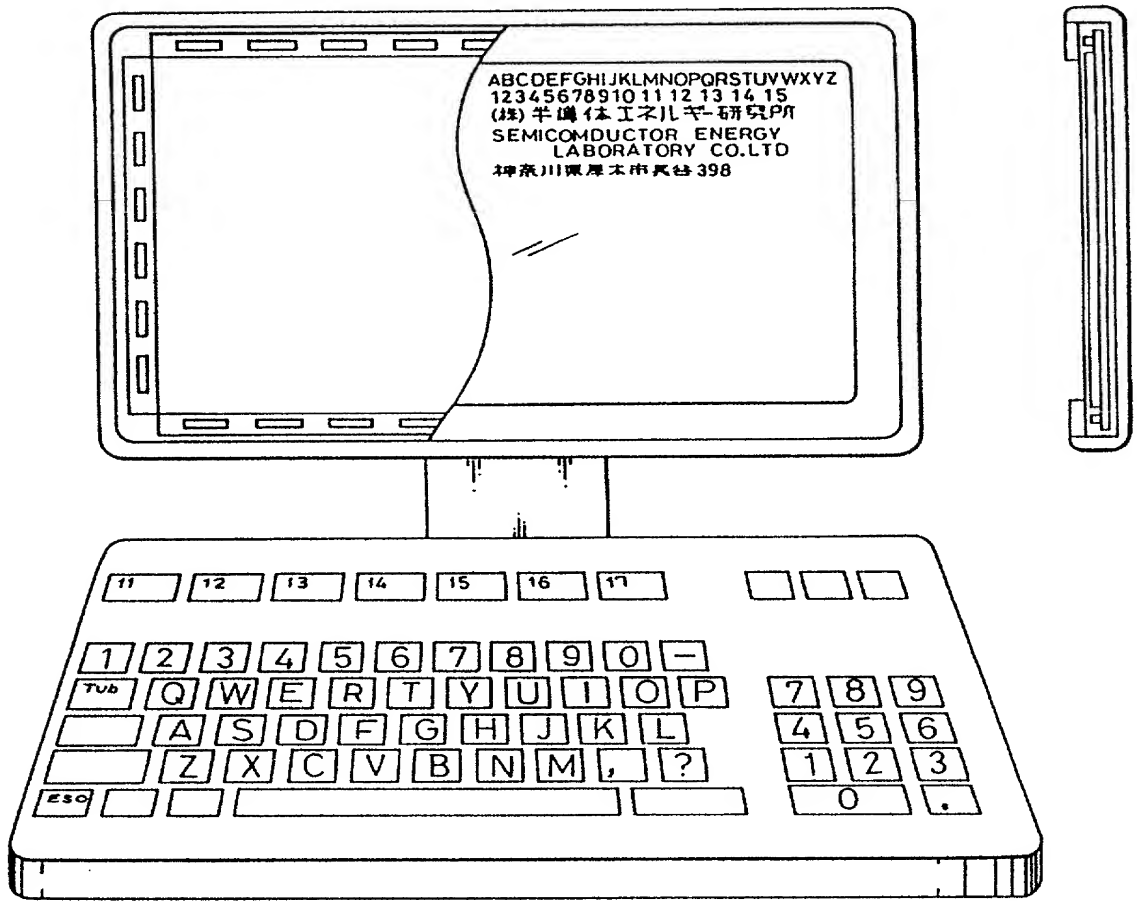

ABCDEFGHIJKLMNOPQRSTUVWXYZ
1234567891011121314 15
(株)半導体エネルギー研究所
SEMICOMDUCTOR ENERGY
LABORATORY CO.LTD
神奈川県厚木市長谷398
11 12 13 14 15 16 17
1 2 3 4 5 6 7 8 9 0 —
Tab Q W E R T Y U I O P
A S D F G H J K L
Z X C V B N M , ?
ESC
7 8 9
4 5 6
1 2 3
0 .

FIG. 21(A)

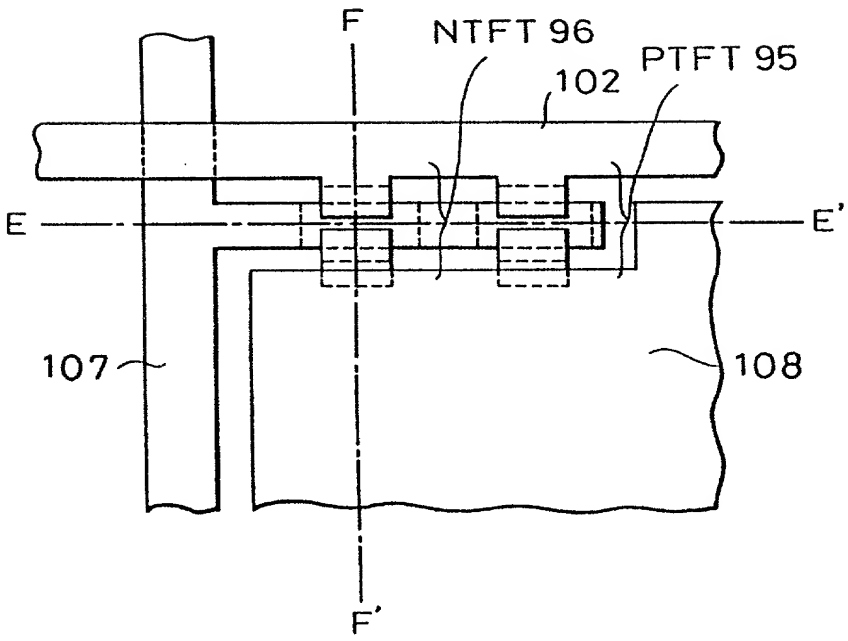


FIG. 21(B)

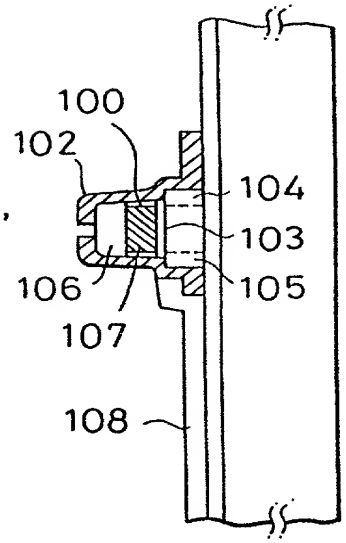
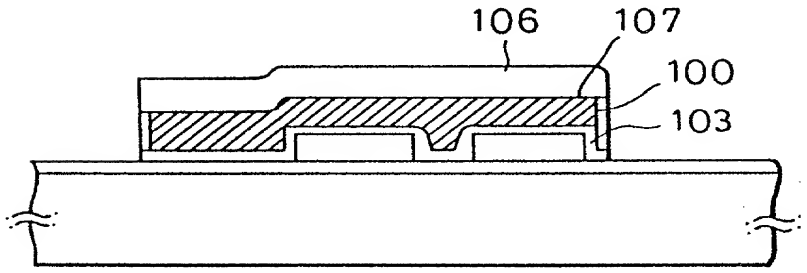


FIG. 21(C)



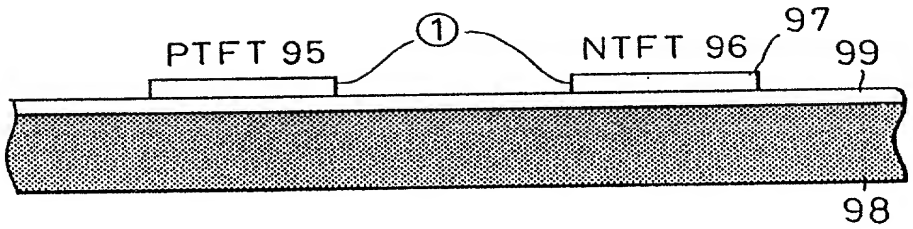


FIG. 22 (A)

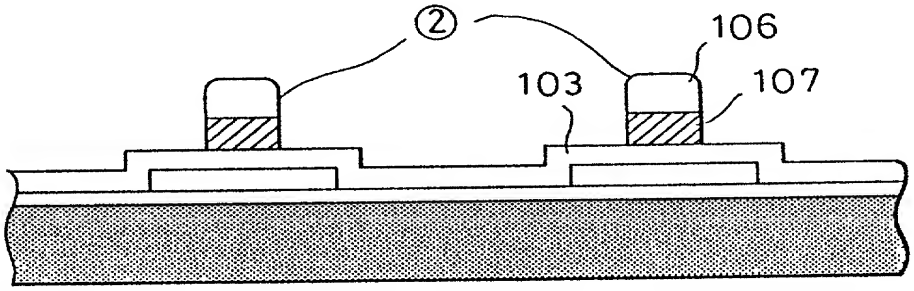


FIG. 22 (B)

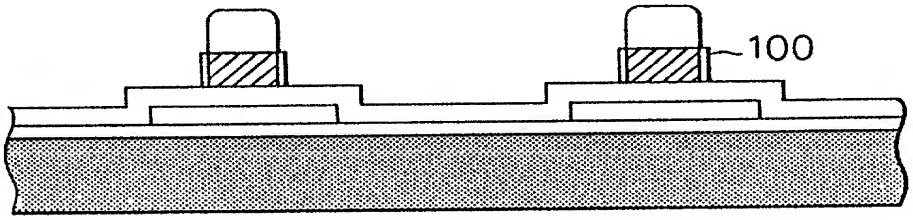


FIG. 22 (C)

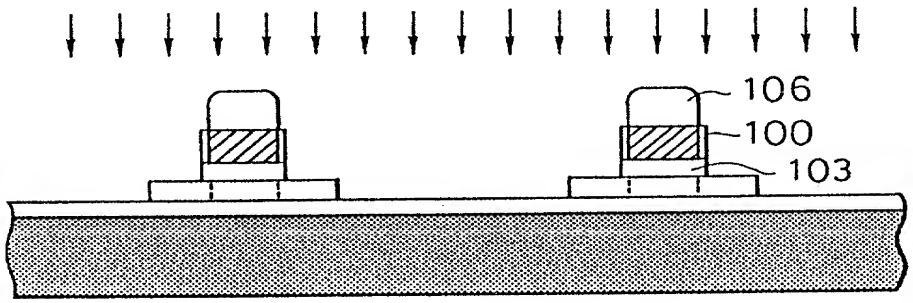


FIG. 22 (D)

FIG. 22(E)

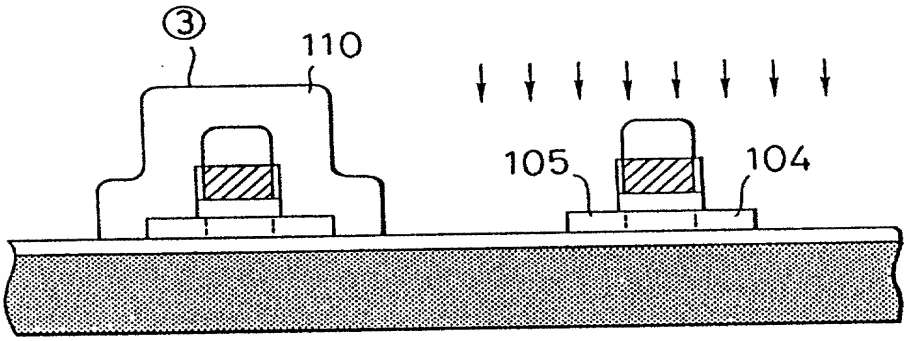


FIG. 22(F)

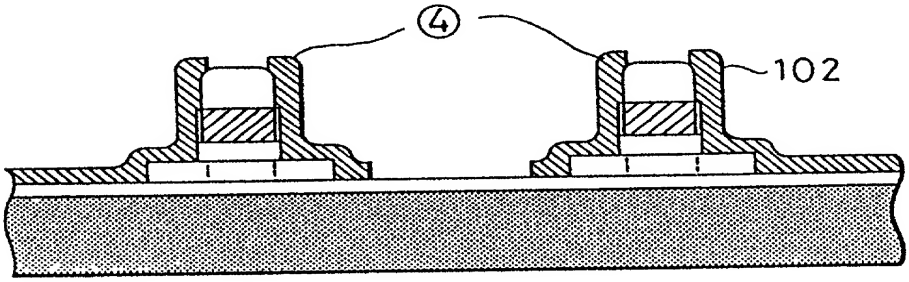


FIG. 22(G)

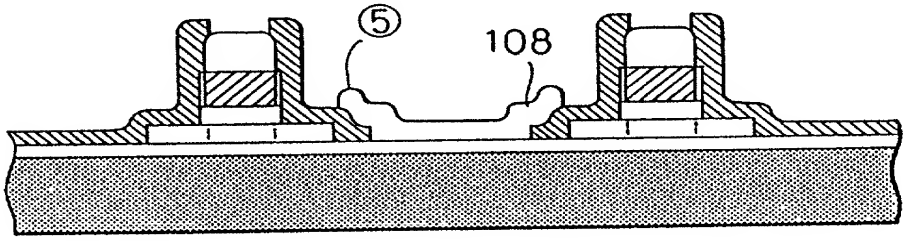
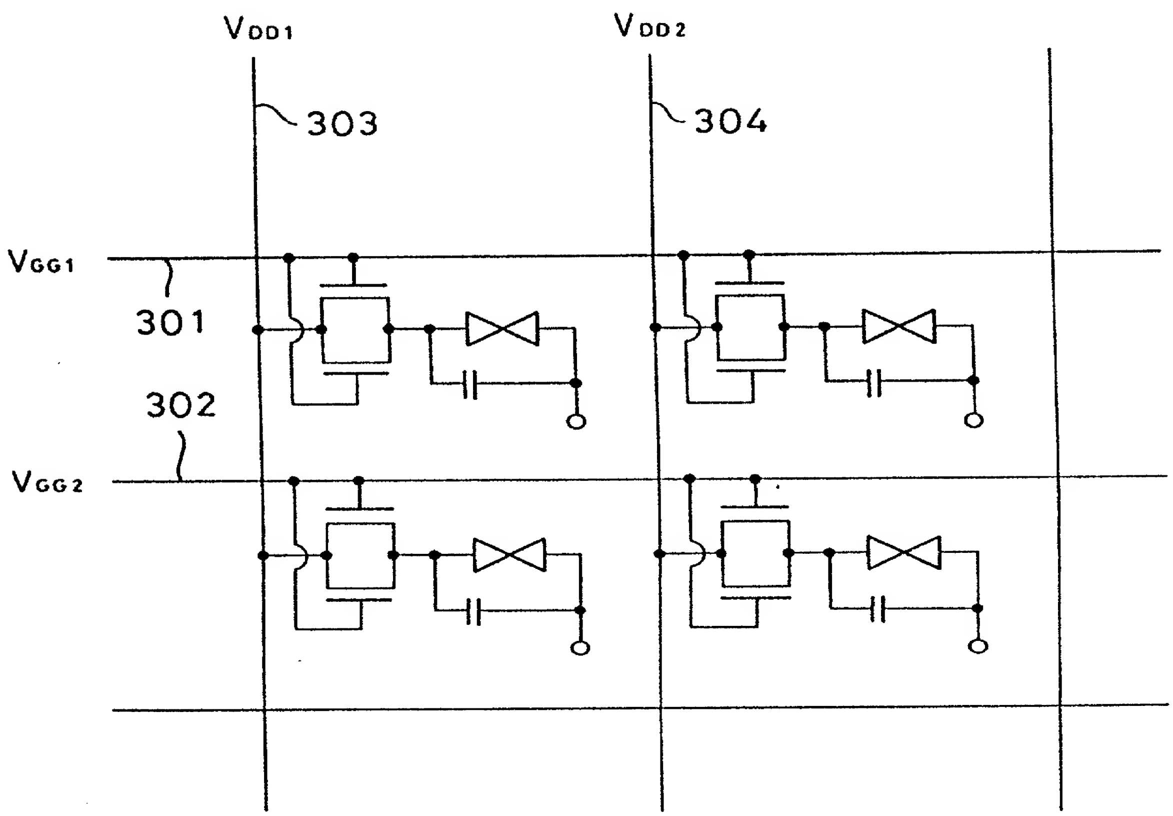


FIG. 23



DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

ATTORNEY DOCKET NO.
0756-718

PLEASE NOTE: YOU MUST COMPLETE THE FOLLOWING:

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the invention entitled: * ELECTRO-OPTICAL DEVICE AND METHOD FOR DRIVING THE SAME

Insert Title

, the specification of which is attached hereto unless the following box is checked:

Check Box If Appropriate — For Use Without Specification Attached

☒ The specification was filed on March 25, 1992
and was assigned Serial No. 07/857,597 (if known)
and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof, or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months prior to this application, and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns, except as follows:

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and checked at right:

Prior Foreign Application(s)

Insert Priority Information (if appropriate)

(Number)	(Country)	(Month/Day/Year Filed)	Priority Claimed Yes	No
3-87780	JAPAN	March 26, 1991	☒	☐
			☐	☐
			☐	☐
			☐	☐
			☐	☐

All Foreign Applications, if any, for any Patent or Inventor's Certificate Filed More Than 12 Months Prior To The Filing Date of This Application:

Country	Application No.	Date of Filing (Month/Day/Year)

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status—patented, pending, abandoned)

Revised 11/90

*NOTE: Must be completed.

I hereby appoint the following attorneys to prosecute this application and/or a international application and to transact all business in the Patent and Trademark Offic connected therewith:

Daniel W. Sixbey (Reg. No. 20,932)
Stuart J. Friedman (Reg. No. 24,312)
Charles M. Leedom, Jr. (Reg. No. 26,477)
Gerald J. Ferguson, Jr. (Reg. No. 23,016)
David S. Safran (Reg. No. 27,997)
Thomas W. Cole (Reg. No. 28,290)

Send Correspondence to:

PLEASE NOTE: YOU MUST COMPLETE THE FOLLOWING

SIXBEY, FRIEDMAN, LEEDOM & FERGUSON, P.C.
2010 Corporate Ridge, Suite 600
McLean, Virginia 22102
Telephone: (703) 790-9110

I hereby declare that all statements made herein of my own knowledge are true and that al statements made on information and belief are believed to be true; and further that thes statements were made with the knowledge that willful false statements and the like so made ar punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the Unite States Code and that such willful false statements may jeopardize the validity of the applicatio or any patent issued thereon.

Insert Name of Non-U.S. firm, attorney or agent

The undersigned hereby authorize any U. S. attorney or agent named herein to accept an follow instructions from Semiconductor Energy Laboratory Co., Ltd. as to any action to be taken in the Patent and Trademark Office regarding this applicatio without direct communication between the U. S. attorney or agent and the undersigned. In th event of a change in the persons from whom instructions may be taken, the U.S. attorneys o agents named herein will be so notified by the undersigned.

Insert Full Name of First or Sole Inventor and Date This Document Is Signed

GIVEN NAME / FAMILY NAME	INVENTOR'S SIGNATURE	DATE
Shunpei YAMAZAKI	Shunpei Yamazaki	5/11/ 1992
RESIDENCE (City, State & Country): Tokyo Japan		CITIZENSHIP: Japanese
POST OFFICE ADDRESS (Complete Street Address including City, State & Country): 21-21, Kitakarasuyama, 7-chome, Setagay-ku, Tokyo 157 Japan		

Insert Residence Insert Citizenship

Insert Post Office Address

Full Name of Second Inventor, if any: see above

GIVEN NAME / FAMILY NAME	INVENTOR'S SIGNATURE	DATE
Akira MASE	Akira Mase	5/7/1992
RESIDENCE (City, State & Country): Aichi Japan		CITIZENSHIP: Japanese
POST OFFICE ADDRESS (Complete Street Address including City, State & Country): 3-75-3, Iga-cho, Okazaki-shi, Aichi-ken 444 Japan		

Full Name of Third Inventor, if any: see above

GIVEN NAME / FAMILY NAME	INVENTOR'S SIGNATURE	DATE
Masaaki HIROKI	Masaaki Hiroki	5/11/1992
RESIDENCE (City, State & Country): Kanagawa Japan		CITIZENSHIP: Japanese
POST OFFICE ADDRESS (Complete Street Address including City, State & Country): 533-10, Shirane, Isehara-shi, Kanagawa-ken 259-11 Japan		

Full Name of Fourth Inventor, if any: see above

GIVEN NAME / FAMILY NAME	INVENTOR'S SIGNATURE	DATE
RESIDENCE (City, State & Country):		CITIZENSHIP:
POST OFFICE ADDRESS (Complete Street Address including City, State & Country):		

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re DIVISIONAL Application of	)	
Shunpei YAMAZAKI et al.	)	
Based On Serial No. 08/912,298	)	Art Unit: 2871
Which Was Filed: July 31, 1997	)	Examiner: J. Dudek
For: ELECTRO-OPTICAL DEVICE AND	)	
METHOD FOR DRIVING THE	)	
SAME	)	Date:

NOTICE OF CHANGE OF ADDRESS

Honorable Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Effective immediately, please note that the address of the attorney(s) of record in the above-referenced application has been changed. Please direct all future correspondence to:

SIXBEY, FRIEDMAN, LEEDOM & FERGUSON, P.C.
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102

Telephone (703) 790-9110

Respectfully submitted,

Eric J. Robinson
Registration No. 38,285

Sixbey, Friedman, Leedom & Ferguson, P.C.
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102
(703) 790-9110